Plasma Processing in the Microelectronics Industry

Bert Ellingboe
Plasma Research Laboratory

Outline

- What has changed in the last 12 years?
- What is the relavant plasma physics?
  - Sheath formation
  - Sheath manipulation
- Advanced plasma processing chamber design
  - TCP vs DFC
- Plasma physics success stories
  - Threshold voltage shifts
  - (Magnetic field effects)
- PRL plans/ what's left to be done?
  - DFC power coupling
  - Plasma current return paths
  - Plasma chemistry

<1 Mbyte design rules

- 5 micron lines and spaces
- 1 micron deep oxide
- >1 micron PR
  - Selectivity of 1:1 OK
- Wet chemistry no longer acceptable

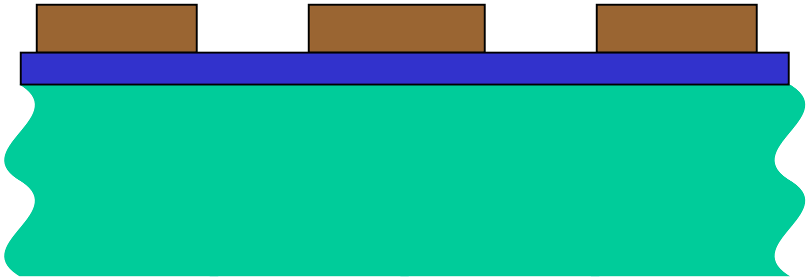
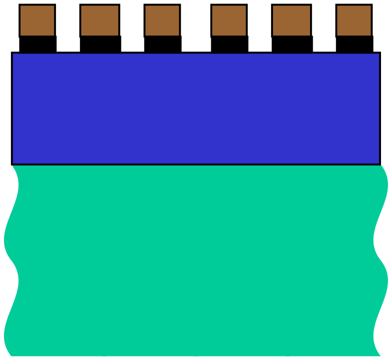
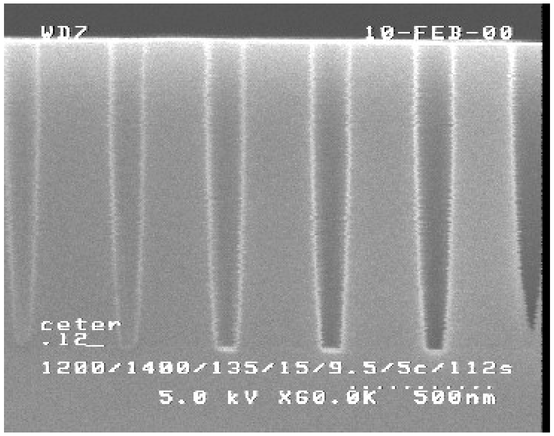


Photo resist
Oxide
Silicon

256 Mbyte design rules; 12 years, 4 gens

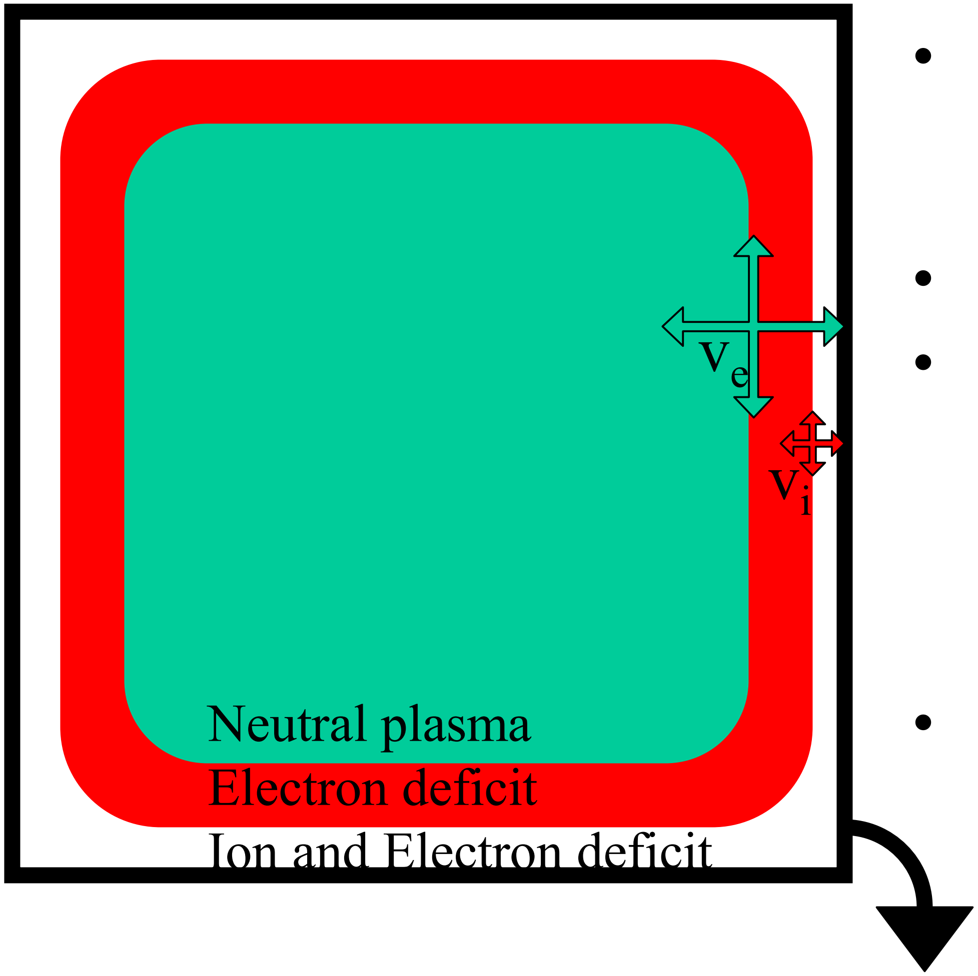


- 0.15 micron lines and spaces, still 1 micron thick (7:1 aspect ratio minimum)
- PR changing, focus on PR
- Dielectric is PR-like
- Added Hard-mask



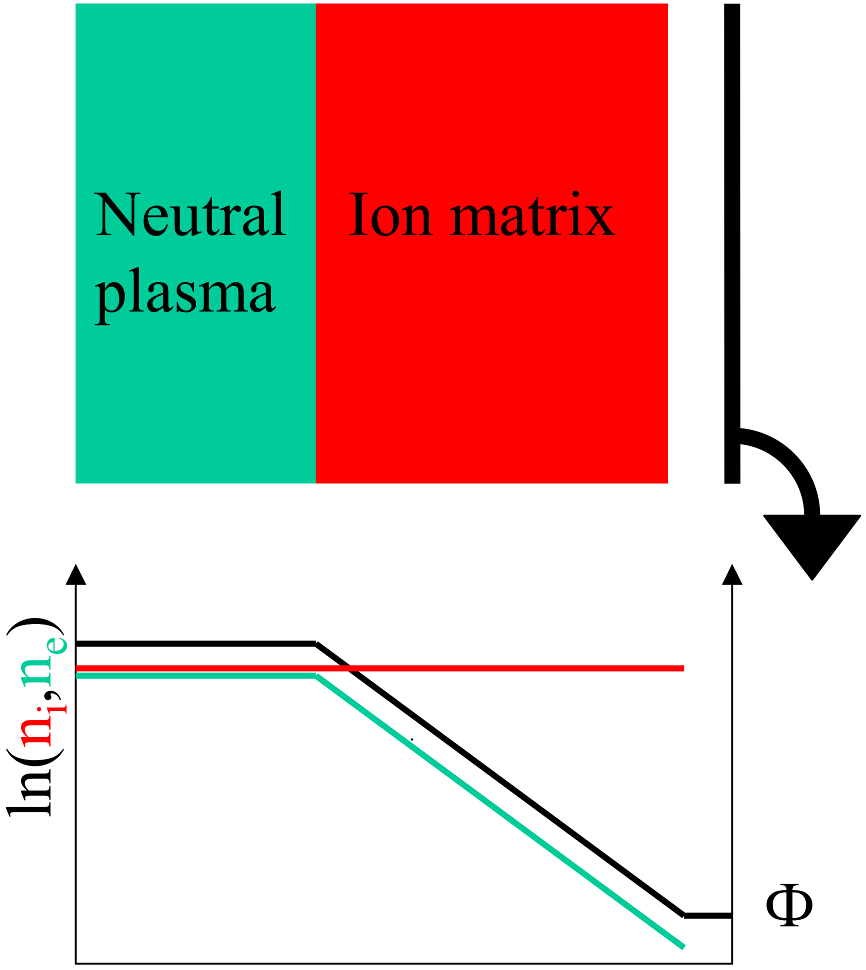
Acceptable etch: 0.20 micron contact, 1.4 micron deep, >88 degree, no undercutting

Basic Low-temperature plasma physics



- Partially ionized (<1%) Plasma filled box (30 mTorr, 1e11/cm^3)
- $T_{wall} < T_i \ll T_e$
- Electron mobility much greater than ion, results in short-time-scale loss of more electrons than ions (absorbed by wall)
- Area of charge imbalance called the sheath

Sheath details



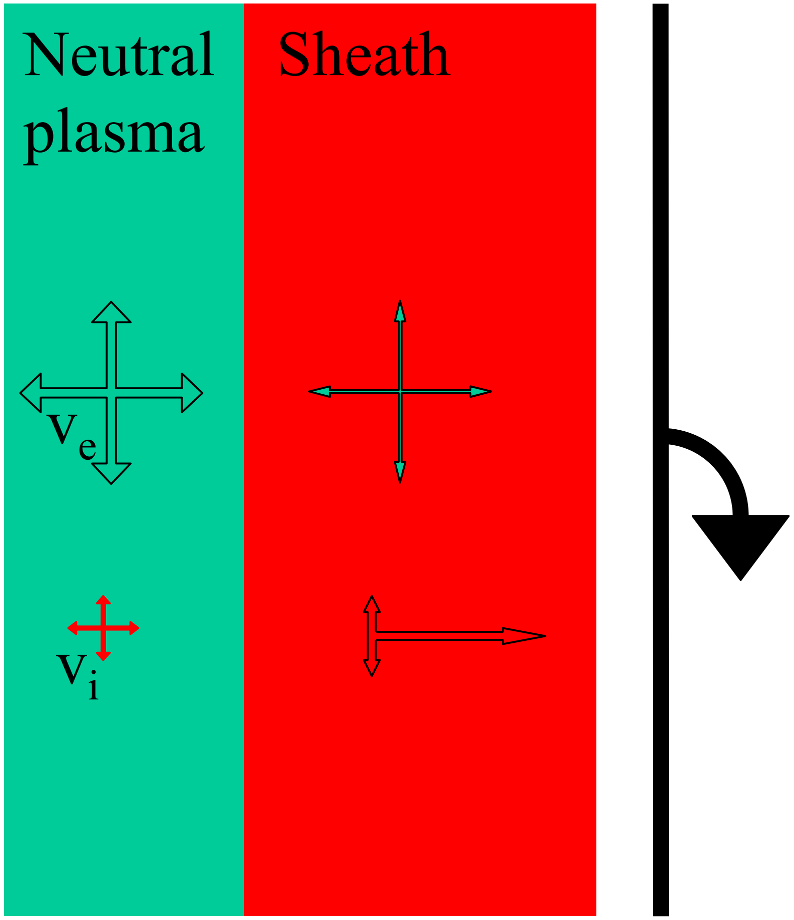
Neutral plasma

Ion matrix

- Electron loss results in excess ions in region of the wall
- Integrating across the free charge gives a voltage which reduces the electron population that reaches the wall.
- Maxwell-Boltzmann

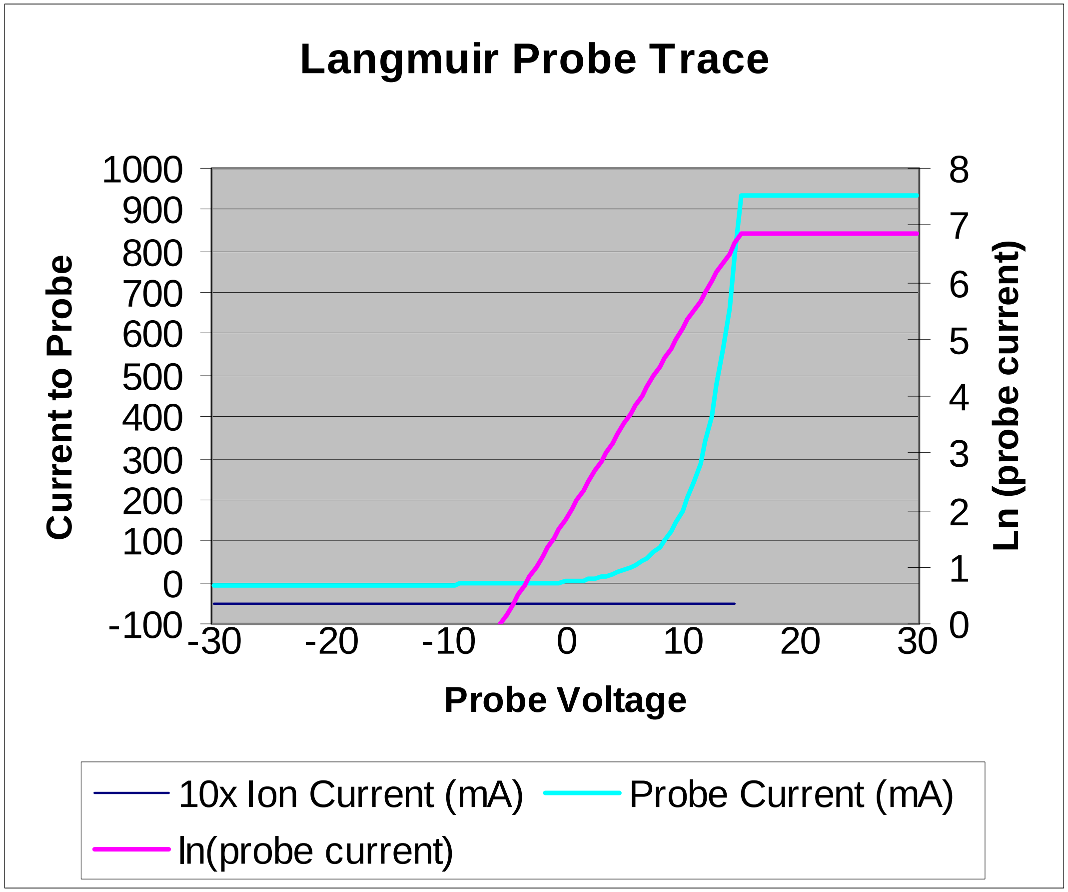
  $n_e(x)=n_{e,0}\exp[(V(x)-V_0)\,/T_e]$

Ion sheath dynamics



- Ions which “wander” into the sheath are accelerated by the sheath voltage and strike the wall with energy equal to the sum of their thermal energy and the sheath voltage.
- The ions fall through the sheath, resulting in super-thermal directed energy *into* the wall.
- Electrons “climb” the sheath, resulting in lower density (Maxwell-Boltzmann $n_e(x)=n_{e,0}\exp[(V(x)-V_0)/T_e]$)

Langmuir probes

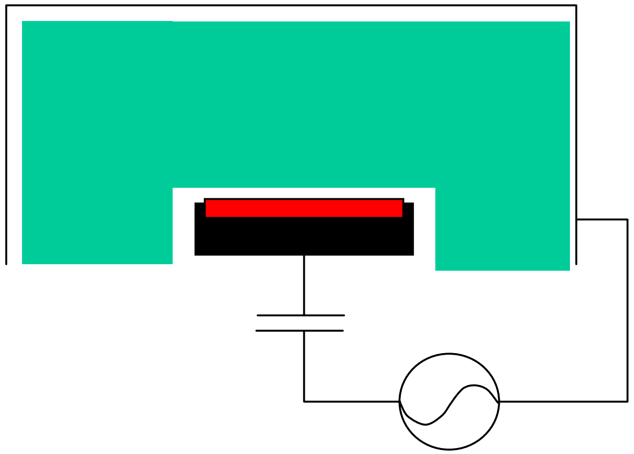


- For a small wire inside the plasma the same sheath dynamics apply
- I-V trace looks as shown on LHS
- Current is the sum of ion (black) and electron currents.

Plasma maintenance

- We use rf power to sustain the plasma
- Frequency is typically between ion and electron plasma frequencies (rf ion motion 90 degrees out of phase with electric field, electron motion in phase with electric field)
  - so electrons respond to the instantaneous field and ions do not.
  - Electrons can be "heated" by the instantaneous rf field

Asymmetric diode

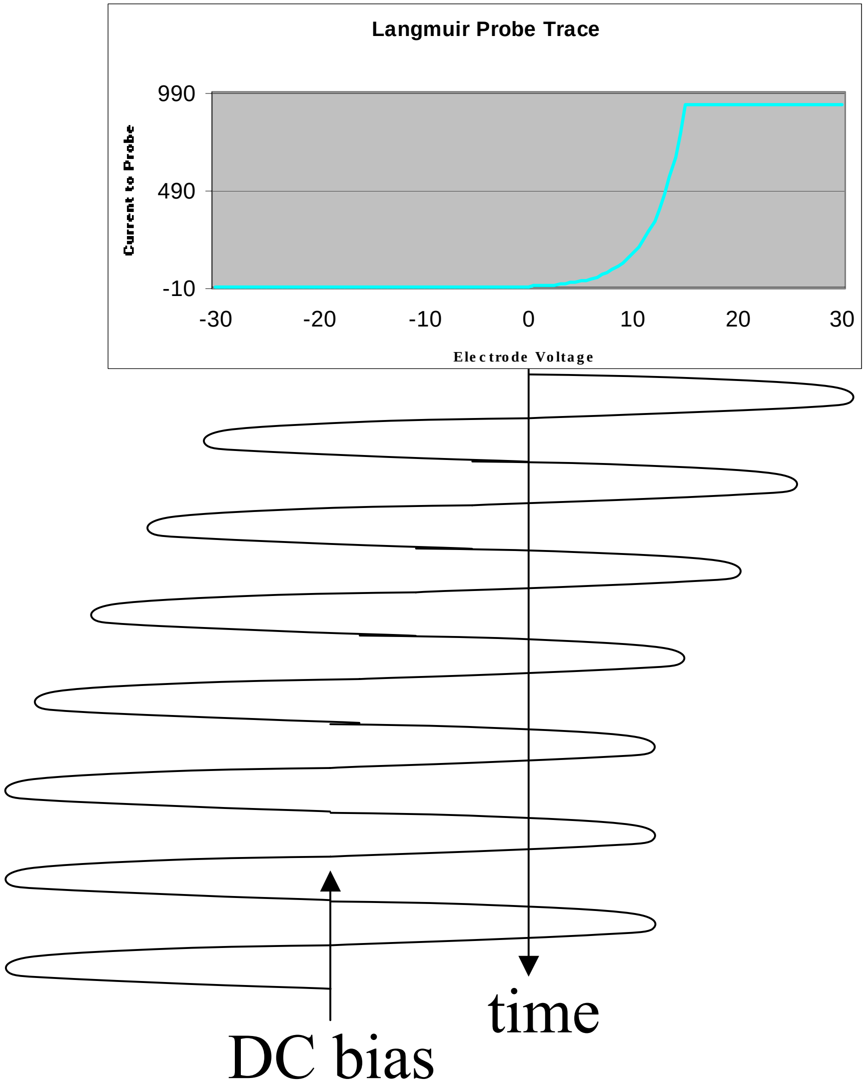


- Small powered electrode with dc blocking capacitor
- Electrode behaves like a langmuir probe
- The capacitor combined with the diode behavior of the sheath results in a time averaged DC bias on the electrode

Development of DC bias

- Blocking capacitor requires zero current over long time scales
- Ion current:
  - Ions respond to time-averaged potential (DC-bias) and are collected uniformly throughout the rf cycle.
  - Ion energy: $E_{ion}=V_p-V_{dc} \cong V_{pp}/2$
- Electrons respond to the instantaneous potential, and are collected only during the small phase during which the electrode potential nears the plasma potential

Development of DC bias

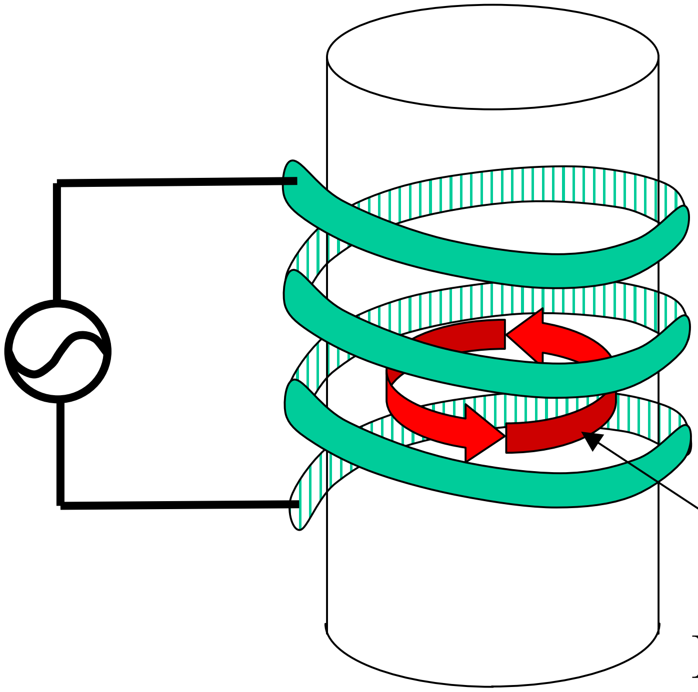


- Blocking capacitor requires zero current over long time scales

- Initial lagrge positive voltage results in electron collection that is not balanced by ion collection, resulting in negative charge on the capacitor

- Ions respond to time-averaged potential (DC-bias) and are collected uniformly throughout the rf cycle.
- Electrons respond to the instantaneous potential, and are collected only during the small phase during which the potential nears the

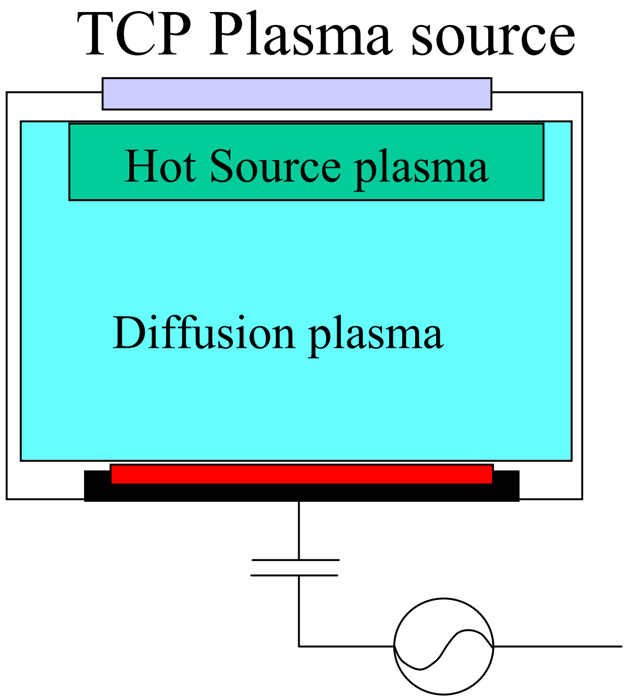
Transformer Coupled Plasma



Quartz tube
filled with
low-pressure gas
(1-100 mTorr)

Plasma current
Image current of antenna
Typical loop-voltage 1Volt

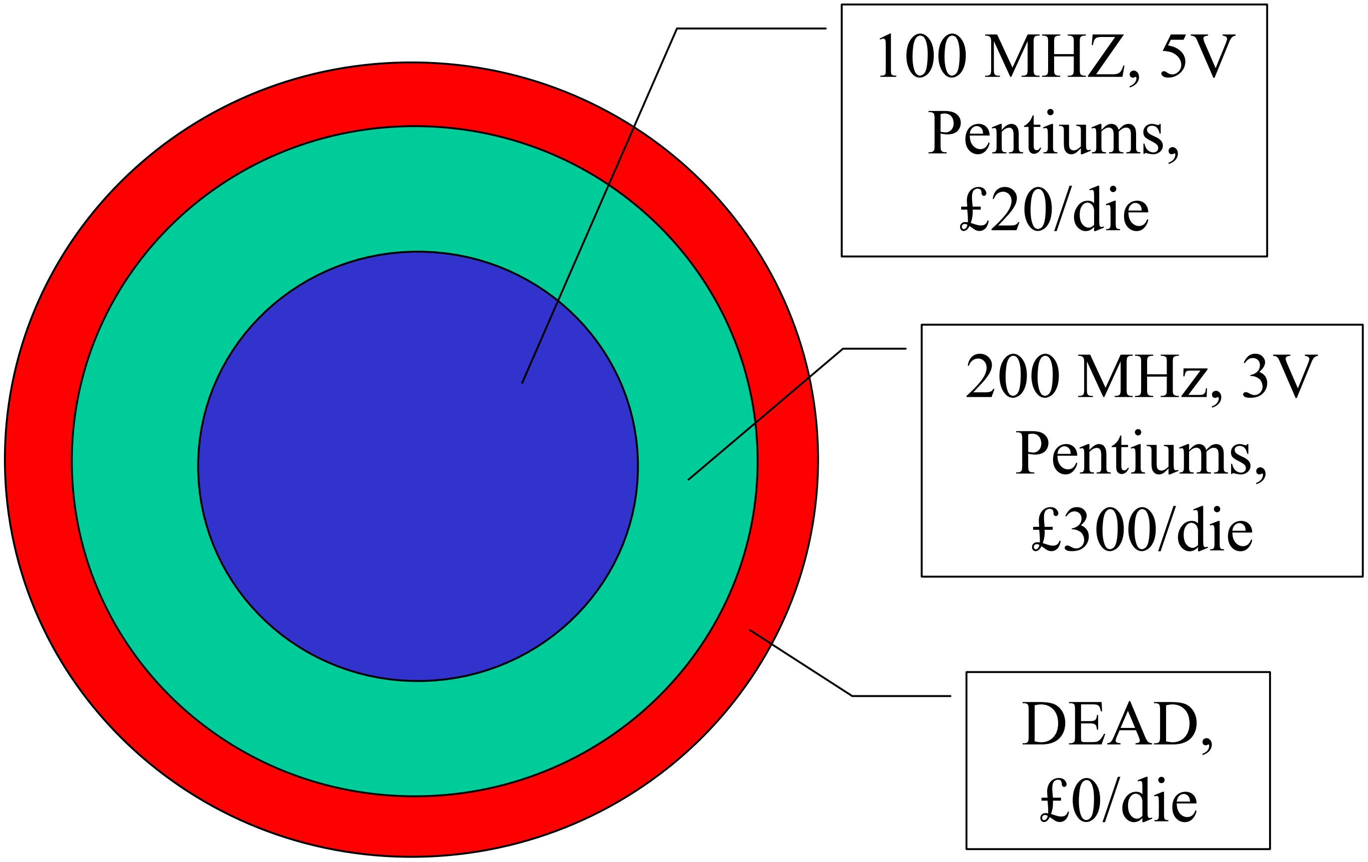
Decoupled plasma sources



- Separation of ion flux and ion energy
- High efficiency plasma source used to determine plasma density and thus ion flux to wafer, with little effect on ion energy
- Capacitive coupled bias used to control ion energy, with minimal contribution to plasma density

Gate threshold voltage shifts due to plasma non-uniformity

- The problem
  - Low voltage devices need tight control of “turn-on” voltage
  - Devices in the center of the wafer had “positive threshold voltage shifts”, and the edge had negative shifts. Due to trapped charge in the gate oxide.



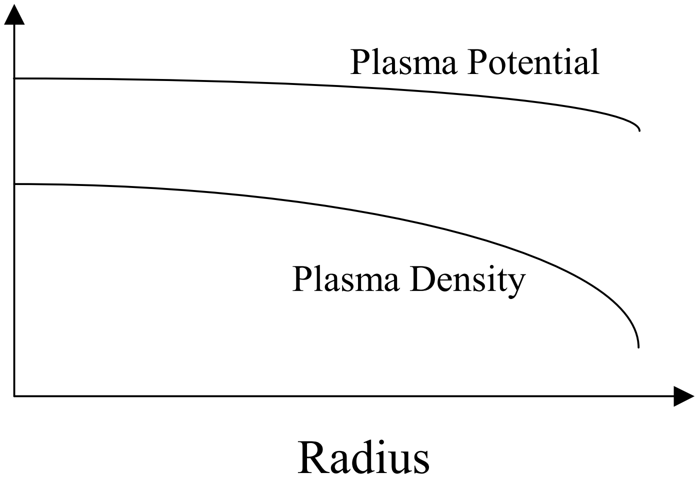
100 MHZ, 5V
Pentiums,
£20/die

200 MHz, 3V
Pentiums,
£300/die

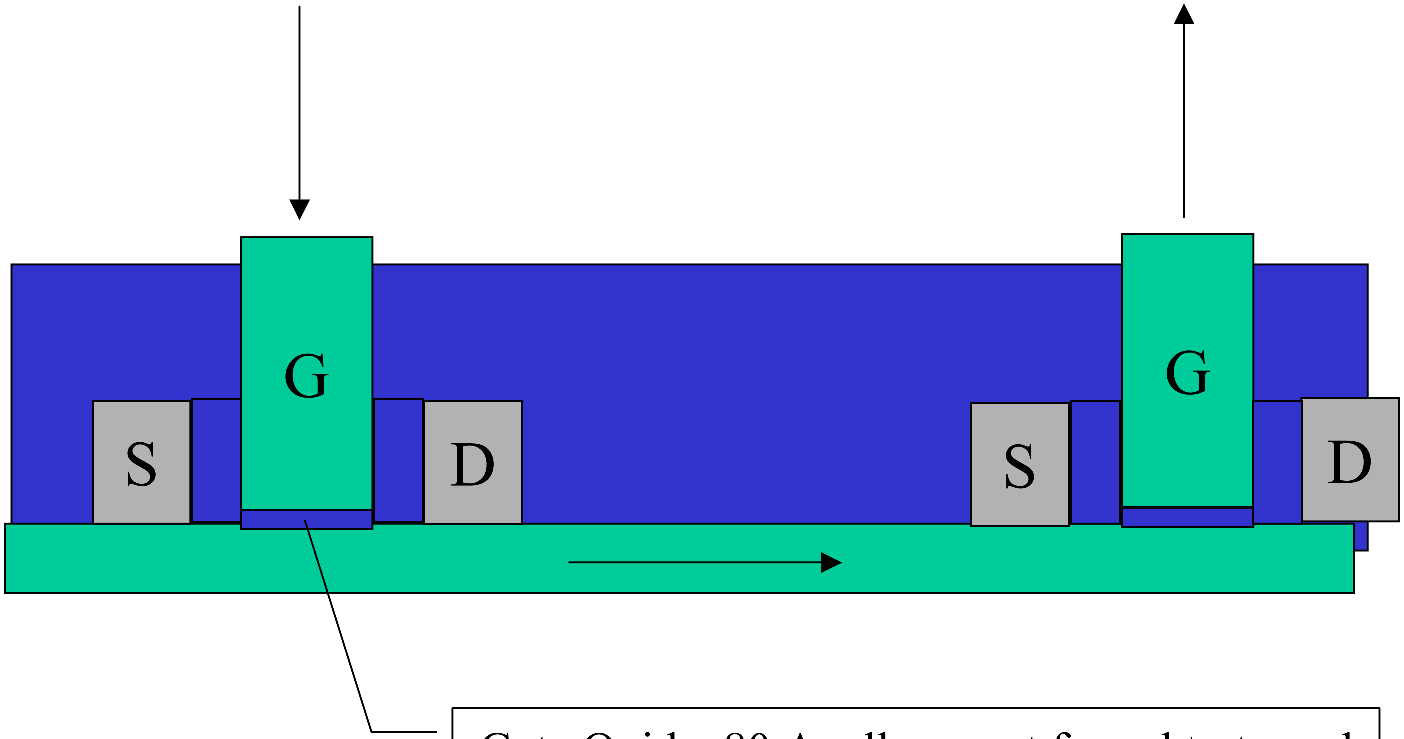
DEAD,
£0/die

Gate threshold voltage shifts due to plasma non-uniformity

- Root cause
  - Diffusion plasma with large separation between source and substrate results in significant radial non-uniformity do to radial diffusion.
  - Because the electrons are Maxwell-Boltzmann, there is a subsequent radial change in the plasma potential. $V_p - V(x) = T_e \ln(n_0/n(x))$
  - This results in excess electrons at the edge of the wafer, excess ions in the center of the wafer, the currents re-connect through the Silicon substrate
  - which results in current through the gates which blows them out.



For the wafer at uniform voltage, outer edge will collect more electrons, since it will be closer to the plasma potential, center of the wafer collects equal and opposite ion current.



Center of wafer, plasma potential high, excess ion current

Edge of wafer, plasma potential low, excess electron current

Gate Oxide, 80 A, all current forced to tunnel through gate oxide, leading to damage

Gate threshold voltage shifts due to plasma non-uniformity

- Solution
  - Use plasma probes to make sure plasma density is uniform.
    - (and thus the market for Scientific Systems was born!)
  - Adjust plasma source power dep profiles to deliver uniform plasma.
    - (and thus 2-D fluid models became important/ prictical – HPEM)

- The real problem: optimized for uniform *etch* by balancing two non-uniformities

Magnetic field effects on local current flux

- ECR plasma source

- MERIE
  - Time averaged uniform plasma and etch rate
  - Time specific gives net current through wafer and blown-out devices.

Present design guidelines

- All surfaces must remain constant over MTBF of tool: 20,000 wafers, 50,000 minutes of processing
  - All surfaces facing the wafer must be kept clean through plasma/chemical/physical bombardment
  - All surfaces must be of “pure” materials
    - Si, SiC, SiN, SiO2
  - Cost of Consumables less than $1/ 300mm wafer equiv.

PRL Plans

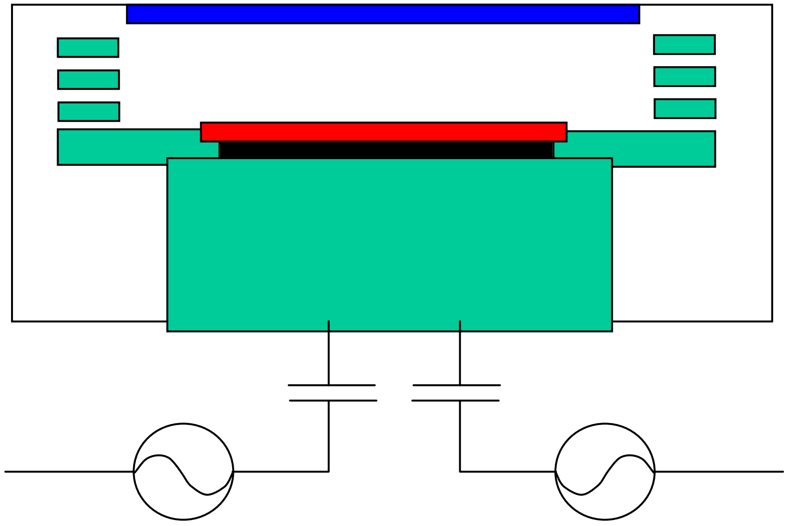
- Basic research
  - ARIS, BARI, and CIRIS experiemnts
  - investigating fundamental phenomena in plasma sources and plasma chemistry
  - Benchmarking plasma modeling codes

- Applied research
  - Exelan DFC (Dual Frequency Capacitive)
    - Separate control of density (ion flux) and energy (drive surface chemistry)
    - Current path from driven sheath to grounded sheath.
    - Roll of each frequency in driving plasma chemistry
  - Lam 9100 TCP
    - TCP plasma with variable return area of capacitive current
    - Coupling between TCP and Bias

Exelan etch chamber by Lam Research

Exelan cross-section

- DFC Chamber
  - One frequency above ion plasma frequencywith some independence in ion energy and flux
- Some independence between ion energy and ion density (current to surface)
- Small volume
  - cheap to have all surfaces facing wafer "Pure"
  - low (variable) gas residence time, control over gas chemistry



lf, couples to ions too

HF, couples to electrons