Unit 58 Circuit simulation using PSPICE

PSPICE is a simulation program for electronic circuits.
Components are connected between numbered NODES in a circuit.
NODE 0 is taken to be ground.
Resistor labels begin with R.
Capacitor labels begin with C.
Inductor labels begin with L.
Silicon transistor labels begin with Q.
Voltage sources begin with V.
Current sources begin with I.
Subcircuit labels begin with X.
.DC analysis applies a swept DC to the named node.
.AC analysis applies a frequency swept AC to the named node.
.TF calculates the transfer function and Thévenin equivalent.
.TRAN analyzes the transient behaviour over the stated time.
.PROBE prepares an output file suitable for graphing.
.END marks the end of the program.

The original SPICE program was written in Fortran by Laurence Nagle for use on mainframe computers and it enabled electronic circuits to be analyzed prior to construction. Detailed mathematical models for actual circuit components were developed and stored in library files. There are student versions of SPICE available at no charge for use on PCs which have a slightly restricted performance. These PC versions are called PSPICE and can be downloaded from the Internet.

The programs listed in this section were developed and tested using version PSEVAL50 of PSPICE. The programs may require some small modifications if later versions are used. The documentation with the version in use should permit the student to carry out any necessary modifications.

There is only one way to learn to use a computer package and that is to sit at the computer and run examples using the package. These example programs show how some of the electronic examples discussed in the text can be modelled using PSPICE. The effects of substituting different values of the components can be explored. It is also illuminating to investigate how the first order approximations which have been used in this text in the explanations of the circuit operation give descriptions of the circuit operation which are close to the circuit performance calculated with the more complete and detailed library models which can use up to 50 parameters to specify the components.

Since there are many tutorial texts available for PSPICE, the programs will be presented without comment. For convenience, the diagrams are repeated here with the programs. The labelling of the nodes should be readily apparent from the component values and circuit diagrams. These programs should be used as a starting point and the component values and analysis types varied to explore the circuit behaviour.

References:

SPICE for Circuits and Electronics using PSPICE, Muhammad Rashid, Prentice Hall (1994).

SPICE A Guide to Circuit Simulation and Analysis using PSPICE, 3rd edn., Tuinenga P. W., Prentice Hall (1995).

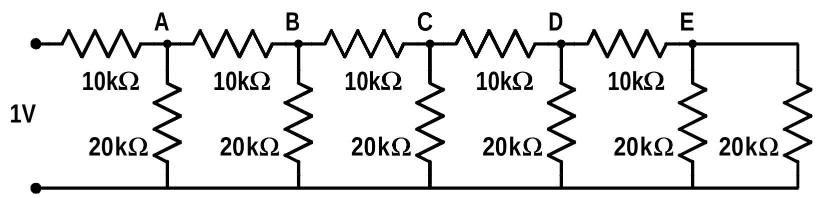

Figure 58.1: Unit 5 Example 5.2.

```
R-2R Ladder
vin 1 0 1
r1a 1 2 10k
r2a 2 0 20k
r1b 2 3 10k
r2b 3 0 20k
r1c 3 4 10k
r2c 4 0 20k
r1d 4 5 10k
r2d 5 0 20k
r1e 5 6 10k
r2e 6 0 10k
.op
.print dc  v(1) v(2) v(3) v(4) v(5) v(6)
.end
```

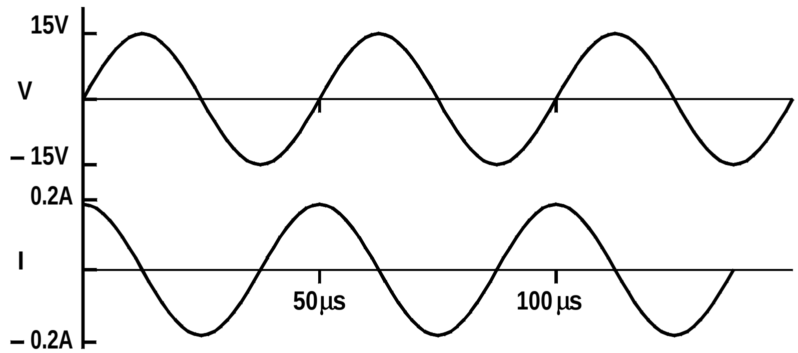

Figure 58.2: Unit 10 Example 10.1 Voltage and current in a capacitor.

```
Unit 10  Example 10.1 Voltage and current in a capacitor
vin 1 0 sin ( 0 15 20kHz )
c1 1 0 0.1uF
.tran 5us 100us
.probe
.end
```

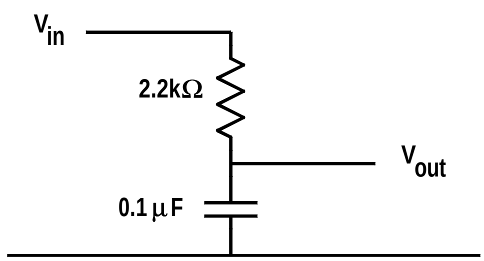

Figure 58.3: Unit 15 Example 15.1 and Unit 16 Low pass filter circuit.

```
Unit 15 Example 15.1 and Unit 16 Low pass filter
vin 1 0 ac 1v
r1 1 2 2200
c1 2 0 0.1uF
.ac  dec 10 10Hz 100kHz
.probe
.end
```

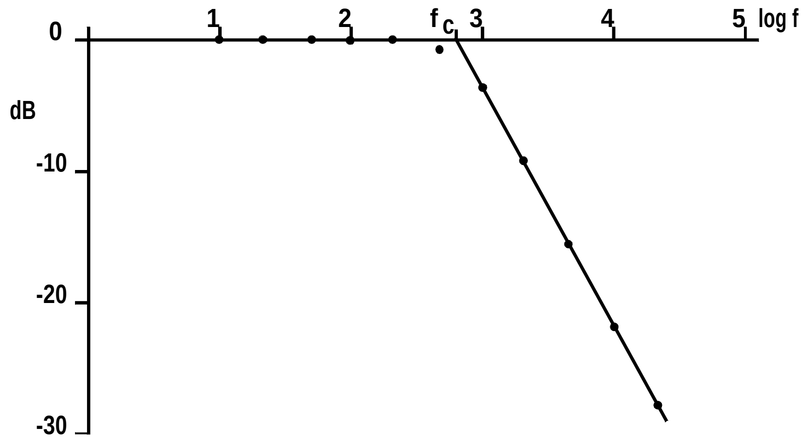

Figure 58.4: Unit 15 Example 15.1 and Unit 16 Low pass filter response.

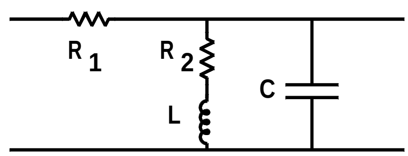

Figure 58.5: Unit 17 Example 17.1 Band pass filter.

```
Unit 17 Example 17.1 Band pass filter
vin 1 0  ac 1V
r1 1 2 1000
r2 2 3 10
L1 3 0 1mH
c1 2 0 0.21uF
.ac dec 20 1kHz 100kHz
.probe  v(2)
.end
```

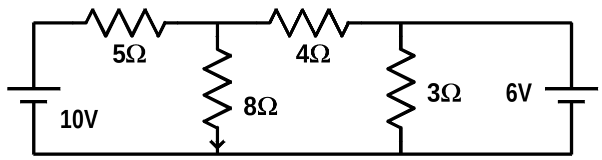

Figure 58.6: Unit 21 Example 21.1 Principle of superposition.

```
Unit 21 Example 21.1 Principle of superposition
va 1 0 10V
vb 3 0 6V
r1 1 2 5
r2 2 0 8
r3 2 3 4
r4 3 0 3
.op
.print dc v(2)  v(3)
.end
```

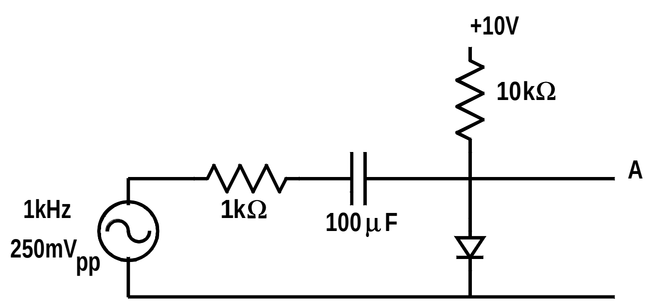

Figure 58.7: Unit 27 Example 27.2 Diode attenuator.

```
Unit  27 Example 27.2 Diode attenuator
vin 1 0 sin ( 0 125mV 1kHz)
r1 1 2 1k
c1 2 3 100uF
d1 3 0 d1N4148
r2 4 3 10k
vdc 4 0 10V
.lib eval.lib
.tran 10us 5ms
.probe v(3)
.end
```

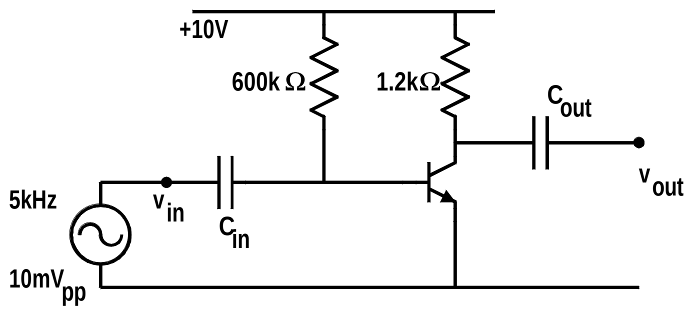

Figure 58.8: Unit 33 Example 33.1 Transistor amplifier.

```
Unit 33 Example 33.1 Transistor amplifier
vcc 1 0 10V
vin 2 0 sin ( 0 5mV 5kHz)
c1 2 3 100uF
r2 1 3 600k
q1 4 3 0 qbc107
r3 1 4 1.2k
c2 4 5 100uF
rload 5 0 1000k
.tran 5us 2ms
.probe
.model qbc107 npn (bf=200)
.end
```

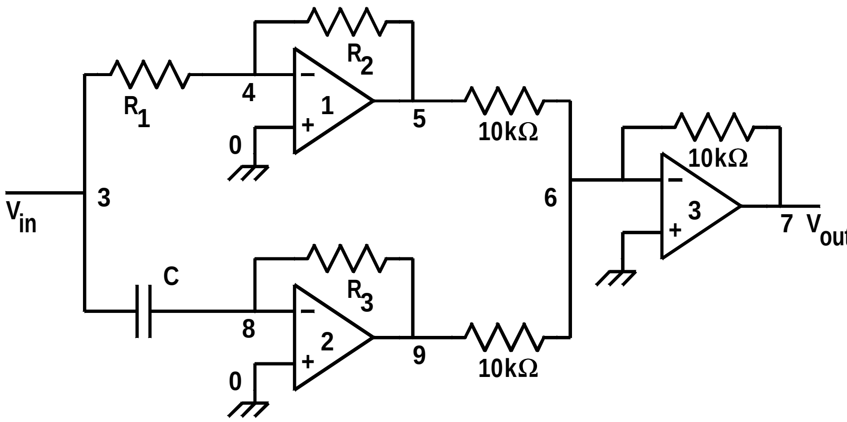

Figure 58.9: Unit 47 Example 47.1 PD controller. PSPICE nodes are numbered.

```
Unit 47 Example 47.1 Proportional plus derivative controller
*Ideal op-amps (Voltage controlled voltage sources) are
*used instead of library ua741 amplifiers.
vin 3 0 pwl ( 0 0 10ms 0  1s 100mv)
r1 3 4 10k
r2 4 5 33k
e1 0 5 0 4 100000
r4 5 6 10k
c1 3 10 1uF
r7 10 8 1000
r3 8 9 2200k
e2 0 9 0 8 100000
r5 9 6 10k
r6 6 7 10k
e3 0 7 0 6 1000000
.tran 5m 1
.probe
.end
```

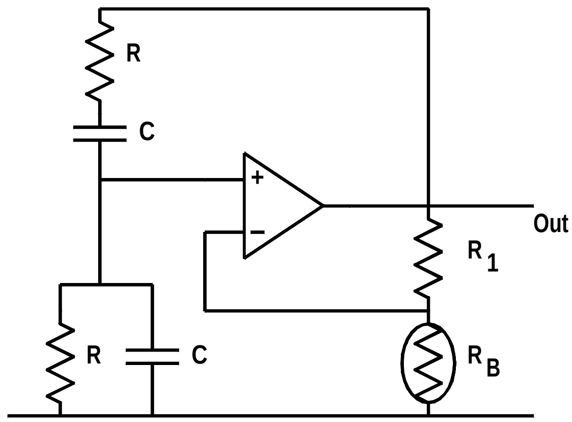

Figure 58.10: Unit 53 Example 53.1 Wein bridge oscillator.

```
Unit 53 Example 53.1 Wein bridge oscillator
vcp 1 0 15
vcn 0 2 15
x1 10 11 1 2 13 ua741
r1 13 4 1000
c1 4 10 1uF
r2 10 0 1000
c2 10 0 1uF
r3 13 11 1000
*Note that Rb is fixed at 400 Ohms
*This gives an exponential growth of the sinusoid waveform
r4 11 0 400
.lib eval.lib
.tran 20us 50ms
.probe
.end
```

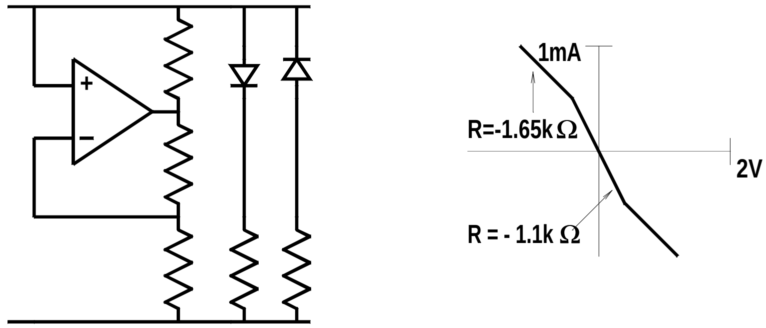

Figure 58.11: Unit 57 The operation of Chua's diode.

```
Chua diode
*negative resistance
vi 4 0  0
r4 4 1 1
r5 1 5 470
r6 5 6 470
r7 6 0 700
v3 10 0 15
v4 0 11 15
x1   1 6 10 11 5 ua741

*nonlinear resistance
r1 1 2 470
d1 2 0 D1N4148
r2 1 3 470
d2 0 3 d1n4148
.dc vi -4 4 .5
.lib eval.lib
.probe
.end
```

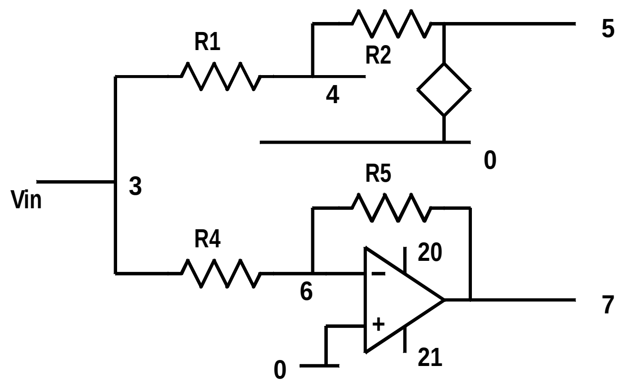

Figure 58.12: Unit 58 Ideal and real op-amps.

```
Test of opamp models
*An Ideal op-amp (voltage controlled voltage source) is
*compared to library ua741 amplifiers
*in inverting amplifier configuration.
vcp 20 0 15
vcn 21 0 -15
vin 3 0 0
r1 3 4 10k
r2 4 5 3300k
e1 0 5 0 4 100000
r4 3 6 10k
r5 6 7 3300k
x1 0 6 20 21 7 ua741
.lib eval.lib
.dc vin -.1 .1 .005
.probe  v(5) v(7)
.end
```