Unit 55 Analog to digital conversion

In an analog to digital converter or AD converter:

- Feedback analog to digital converters include a DA converter.
- An algorithm is used to drive the DA converter which gives one of:
  - Ramp type conversion
  - Tracking conversion
  - Successive approximation
- Flash converters carry out the conversion at high speed using a resistor network and a bank of comparators.
- Integrating converters integrate the input voltage for a fixed time and then measure the time required to restore the output of the integrator to zero using a negative reference voltage.

There are many different analog to digital converters available. The Analog Devices *Data Conversion Products Databook* lists approximately 50 different families of AD converters. In all cases the device is used to obtain a digital value for an analog voltage presented at the input to the IC.

There are many features considered in the design of AD converters, such as accuracy, speed of conversion, price, compatibility with computer interfaces, linearity, precision, noise rejection, and it is compromises in the emphasis on these various features that lead to the wide range of available devices.

We will therefore not cover all of the available families of devices but rather look at the three broad groups of AD converters and see how they operate and try to see why certain families are better suited for certain applications.

Feedback analog to digital converters. This approach to AD conversion uses the digital to analog converters discussed in Unit 54 and incorporates them in a feedback system such as that shown in block diagram form in Figure 55.1.

A digital logic unit (DLU) generates an 8 bit binary number according to some algorithm. This number is fed to a digital to analog converter which

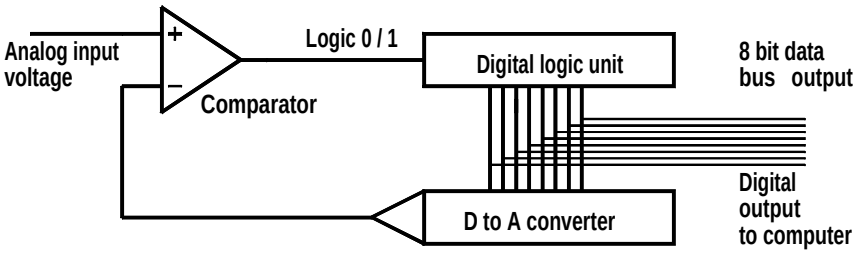

Figure 55.1: Block diagram of feedback AD converter.

generates the corresponding analog voltage and feeds it to a comparator. The comparator is basically an op-amp which is used without feedback and which has two output states: an output of 0 V or logical 0 when the inverting input is less than the noninverting input and an output of +5 V or logical 1 when the inverting input is greater than the noninverting input. The comparator output is fed to the DLU and controls the execution of the algorithm.

The system attempts to match the output of the digital to analog converter to the analog input voltage to within the resolution of the DA converter. The logical output of the comparator both determines the accuracy of the match and also controls the DLU in achieving a match. When a conversion is complete, the output of the DLU is also put on the 8 bit data bus output from which the data is read into the computer.

There are three basic types of algorithm or program which are programmed into the DLU by the manufacturer of the feedback AD.

A ramp type conversion algorithm is shown in Figure 55.2.

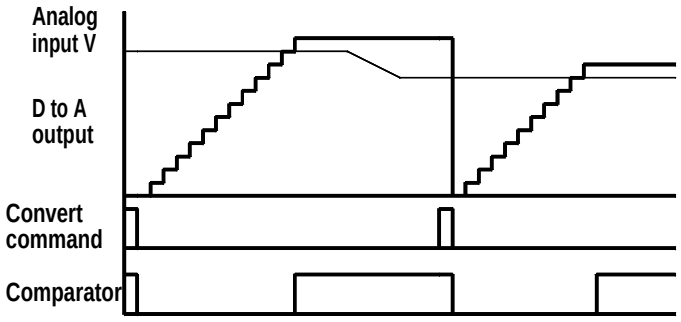

Figure 55.2: Ramp type feedback converter.

The DLU is programmed to operate as a counter which counts the cycles of a clock. The output of the counter is fed to the DA and the output of the DA therefore ramps up, or in fine detail moves up the voltage staircase, until the comparator changes state. At this point the clock input to the

comparator is stopped and the count or data is read into the computer. In many cases the comparator output is also fed to the computer to signal the end of a conversion which signals that the data on the bus is now a valid representation of the AD conversion output and can be read by the computer. When the main computer determines that a reading is to be made, a conversion or measurement is initiated by putting a pulse on the convert command line as shown in Figure 55.2.

The second algorithm used in feedback AD conversion is the **tracking converter** for which the operating configuration is shown in Figure 55.3.

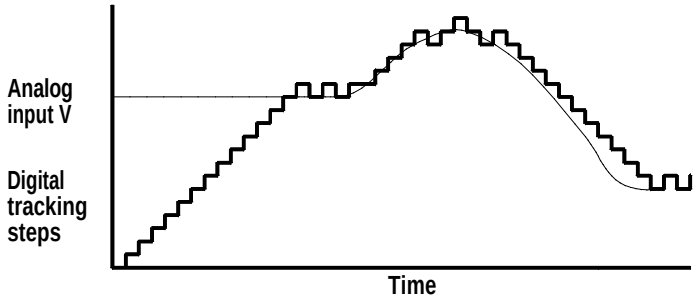

Figure 55.3: Tracking type feedback converter.

Initially this operates as a ramp type converter but it does not stop as soon as the point is reached where the comparator triggers, but rather the counter is switched from count-up mode to count-down mode so that the DA converter output continually brackets the analog input voltage. If the analog input voltage changes then the DA converter tracks it by taking more steps up than down on an increasing input voltage. The limitation of the system shows up when the analog input voltage changes at a rate faster than the maximum rate of the ramp or staircase as shown for a short segment of the falling edge of the sample shown in Figure 55.3.

Tracking type AD converters can also be used with 16 bit systems for digitizing audio signals in the preparation of masters for compact disks. The 16 bit digitizing resolution corresponds to the 100 dB dynamic range of hearing. The advantage of the tracking system is that it avoids the necessity for storing $44.1 \times 10^3 \times 16$ bits or 0.7 megabits of data per second of recorded sound when a sampling rate of 44.1 kHz is used.

Since the analog signal tends to be continuous, there is no point in going back to zero each time a conversion is required. Also, in audio signal digitization what is important is not the absolute pressure value on the microphone but rather the changes in the pressure, the sound, as recorded by the microphone.

In order to digitize an audio waveform, a sampling rate in excess of 20 kHz

is required. If a 12 bit AD converter is used the data rate is then 20 kHz×12 = 240000 bits per second which is greater than the available bandwidth in audio systems. In the tracking AD converter, only the changes need to be transmitted so the transmitted or recorded signal is a bit stream representing up or down steps. When conversion back to analog is required, a single bit DAC is used. A simplified representation of this converter is shown in Figure 55.5. A stream of logic 0 or 1 bits, representing the up and down steps from the tracking converter, are level shifted to -5 V and $+5$ V and applied to the gates of the two complementary MOSFETs so that the input to the integrator is connected to -5 V for a 0 bit or to $+5$ V for a 1 bit. The integrated and smoothed output then forms the analog signal for playback. The integration time is about 50 μs to allow rapid tracking of the signal.

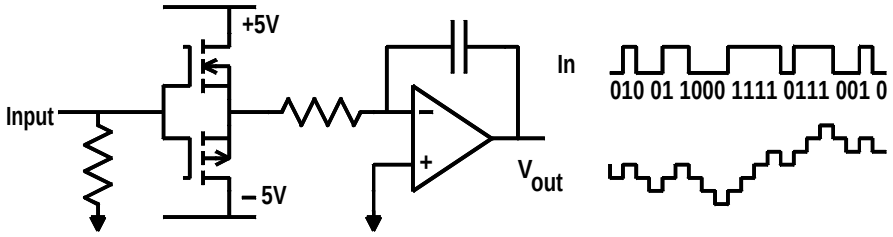

Figure 55.4: Principle of operation of single bit DAC.

The third type of feedback AD converter is the **successive approximation** type of converter. The strategy used in this conversion is the same as that used in the game where player A writes down a random number between 1 and 1000 and player B has to determine the number by guessing a value for the number and asking player A if the guessed value is the value written down. The most efficient strategy for B is to start with an initial guess of 500. If the reply is 'too low' then the next guess should be $500 + \frac{1}{2} \times 500 = 750$. If the reply is 'too high' then B takes away the increment and adds on half of the increment to guess $500 + \frac{1}{2}250 = 625$. At each stage the range of possible values is reduced by a factor of 2. This algorithm, as applied to a feedback AD converter, is shown in Figure 55.5.

The input signal is fed through a sample and hold amplifier to prevent the value changing while the conversion is being carried out. This sample and hold is not shown. The momentarily constant input voltage is shown as a fine line on the graph and marked Analog input V. Initially all 8 bits at the output of the DLU are set to 0. In the first time interval, the most significant bit of the DA converter is set to a 1. The result of the comparison is that $V_{in} > V_{DA}$ and therefore the 1 bit is left in position. In the next time interval the next most significant bit is set to 1 and the result of the

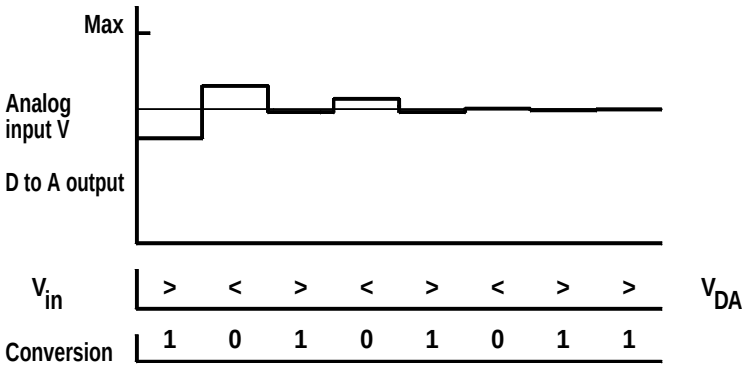

Figure 55.5: Successive approximation type feedback converter.

comparison is that $V_{in} < V_{DA}$ so that the bit is reset and a 0 is placed in the position.

Thus, in eight time intervals, it is possible to carry out an 8 bit conversion to an accuracy of 1 part in 2^8 or 1 part in 256. The minimum time interval is determined by the settling time of the DA converter and the comparator and may be of the order of $2\,\mu$s. So a typical AD conversion and data readout using this system can be carried out in about $20\,\mu$s making this one of the faster types of AD converter.

A flash converter is shown in block diagram form in Figure 55.6.

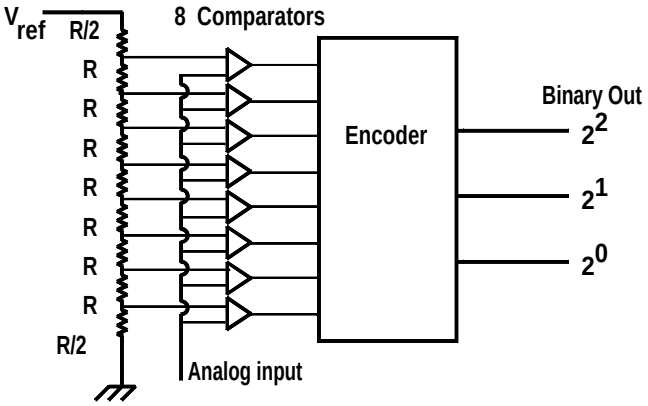

Figure 55.6: Flash type AD converter.

In this 3 bit converter, a resistive network consisting of seven resistors of value R (typically $10\,\text{k}\Omega$) and the top and bottom resistors of value $\frac{1}{2}R$ are used to give eight voltages over the range from 0 V to the reference voltage, V_{ref}. The analog voltage input is simultaneously compared with each of these tapped off voltages in a bank of eight comparators. The logical outputs of these eight comparators are fed to an encoder which generates an output

binary number which is the number of the lowest untriggered comparator.

The fact that the system operates in parallel on all comparators means that its speed is limited only by the comparator operating speed and therefore this system is used for very high speed operation such as digitizing television and video signals in real time. One line of a TV picture lasts 64 μs and requires about eight conversions per microsecond to give 500 pixels across the screen. The system shown in the figure is a 3 bit system of low resolution. An 8 bit system utilizes $2^8 = 256$ comparators and is a fairly substantial piece of electronics. It is normally installed as a card within a computer to minimize the time associated with the transfer of high speed data through the system or along cables. The complexity of the electronics is also matched by the cost of the converter and the cost of computer memory: 1MByte of memory is filled for each four digitized images at a 500×500 pixel resolution. Given that images are updated at a rate of 25 per second in a video system, a lot of expensive memory can be filled very quickly!

So in general, flash converters have a specialized range of application in digitizing very high speed events and in digitizing images which warrant the high system costs.

Integrating AD converters. These converters are widely used in digital multimeters. The basic block diagram of the converter is shown in Figure 55.7.

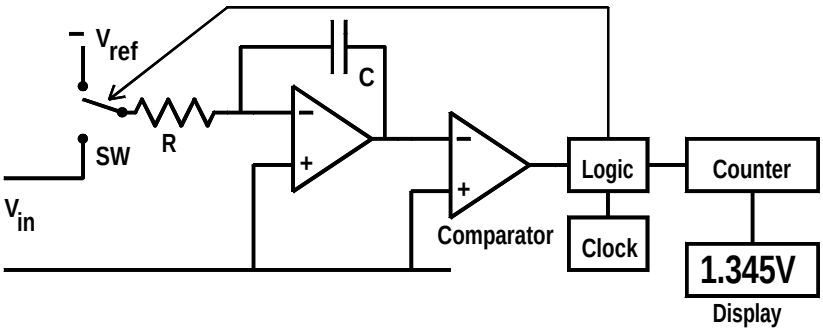

Figure 55.7: Block diagram of integrating type converter.

An input voltage is integrated for a fixed time in an op-amp integrator having a time constant CR. At the end of the time interval, T_{int}, the input voltage is disconnected from the integrator and a negative reference voltage is switched to the input to the integrator. This results in the output of the integrator returning towards zero volts. The time when this occurs is determined by a comparator and the time taken for the integrator output to be brought back to zero is recorded in clock cycles in a counter. Appropriate scaling of the R and C gives a count which is numerically equal to the input voltage.

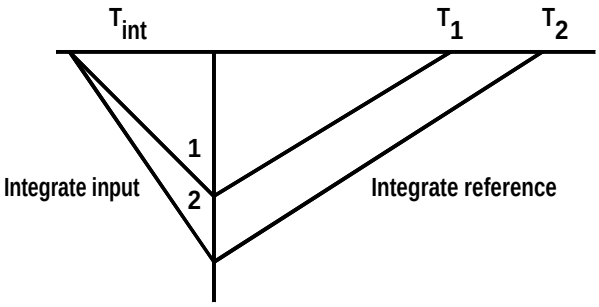

Figure 55.8: Operation of integrating type AD converter.

Figure 55.8 shows the voltages at the output of the integrator due to two different input voltages V_1 and V_2 being integrated for the fixed time interval T_{int}. The output voltage reached is greater for the larger input voltage V_2. When the switch is changed over to the reference, the rate of change of the integrator output is the same for the two measurements but T_2 is longer than T_1. The integrator therefore converts a voltage measurement to a time measurement: $T_n \propto V_n$. The values C and R are not critical. It is only required that they do not change during the short measurement time because they are used in both the integration of the input signal voltage and also in the integration of the negative reference voltage. The reference voltage does affect the accuracy of the scaling but this single component can be fabricated to the required high accuracy. The integration time is usually made to be equal to the period of the mains frequency so that any spurious pick-up of mains voltage will average to zero over a full cycle.

One chip normally contains the op-amp, comparator, clock and the liquid crystal display driver circuits and mass production gives the high accuracy, low cost hand held meters which are in use in all laboratories in large numbers.

55.1 Problems

55.1 What is the resolution in volts of a 12 bit AD converter with a range from 0 V to +5 V?

55.2 What is the binary output of an 8 bit converter with a range from 0 V to +10 V for input voltages of +1.3 V, +4.3 V and +8.2 V?

55.3 What is the average conversion time of an 8 bit ramp type converter in which a 10 kHz clock is used?

55.4 Draw a flow chart for a program to control the operation of the successive approximation feedback converter shown in Figure 55.5.