Unit 54 Digital to analog conversion

In a digital to analog converter or DA converter:

- A resistive ladder is used to give successive fractions of a reference voltage.
- Each divided down voltage fraction drives a current, proportional to the voltage, through a resistor.
- The current through the resistors can be switched to the input of a current to voltage converter.
- The current to voltage converter sums all of the switched currents to generate a voltage output proportional to the binary value of the switches.

In analog electronics we deal with continuously variable quantities such as current or voltage which can have any value within a permissible range. These voltages or currents can then be used to represent continuous real world variables such as position, velocity, pressure, light intensity etc.

In digital electronics, quantities are represented by numbers which are themselves represented by discrete voltage levels. Since much of modern technology is based on the use of digital computers, it is necessary to have methods of obtaining an analog output from a digital computer (DA conversion) so that computers can exercise control over the external world and also it is necessary to have methods of obtaining a signal in digital form which is compatible with digital computers (AD conversion) and which represents the conditions in the continuously variable real world.

Digital computers carry out calculations in binary arithmetic, that is using a number system where the digits are 0s and 1s. The position of the digit is used to represent the significance of the number so that a conversion from binary to digital representation would be:

$$00101101_{Binary} = 1 \times 2^5 + 0 \times 2^4 + 1 \times 2^3 + 1 \times 2^2 + 0 \times 2^1 + 1 \times 2^0 = 45_{Decimal}$$

In order to represent this binary number in electronics, a bus, typically of eight wires in parallel, would be used in which a 0 V signal on the wire represents a logical 0 in the corresponding position of the binary number and a 5 V on the wire represents a logical 1 in the corresponding position of the binary number. The binary equivalent of 45 decimal, when placed on an 8 bit bus, would give the voltage configuration shown in Figure 54.1. The terms msb and lsb represent most and least significant bit.

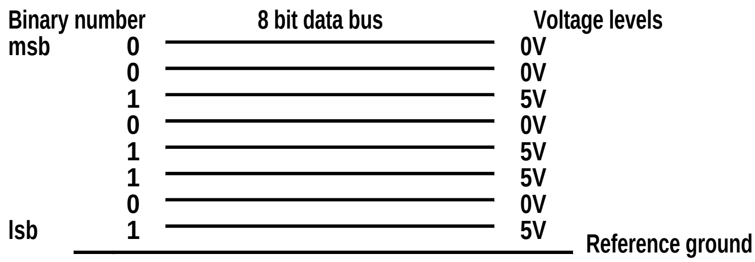

Figure 54.1: Binary number and corresponding voltage levels on the bus.

For simplicity, we will discuss digital to analog conversion in terms of 8 bit data buses but higher resolutions of 12, 14 and 16 bits are frequently used. In a DA conversion we convert the voltage levels on the eight wires of the bus into a single voltage level at a single analog output.

First, we set the range of the output. Typically this would be from 0 V to 1 V but it is straightforward to change the scale. The 8 data bits correspond to a range from 00000000 to a maximum of 11111111 in binary which corresponds to a range from 0 to 255 in decimal. So instead of an analog voltage which varies continuously from 0 V to 1 V we can only generate a set of 256 discrete values spaced at intervals of $\frac{1}{256} = 3.9\,\mathrm{mV}$ apart. The resolution of the system is said to be 3.9 mV. Greater resolution is obtained by using more bits and a larger range of binary number.

The problem of D to A conversion has now been reduced to this: given eight wires going into a converter circuit, with voltage levels on these wires representing an 8 bit binary number, how can a voltage be generated at the output of the DA converter which is proportional to this binary number?

Many conversion systems have been developed but there is one system which is most commonly used called the R–$2R$ ladder converter.

Consider the circuit shown in Figure 54.2 (a). We have a reference voltage, V_{ref}, which is typically 1 V and is applied across a potential divider of R and two $2R$ resistors in parallel. This is equivalent to the potential divider of two equal resistors as shown in Figure 54.2 (b). The voltage at the centre of the potential divider is then $\frac{V_{ref}}{2}$. In Figure 54.2 (a), one of the $2R$ resistors is grounded at the bottom. The other $2R$ resistor goes to the switch and is either grounded or fed to the inverting input of a current to voltage converter circuit. Using the op-amp rules (Unit 39) the voltage at the inverting input is

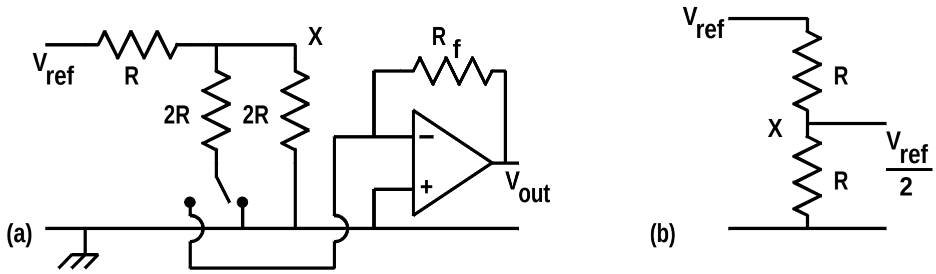

Figure 54.2: Single unit of R–$2R$ ladder network.

equal to the voltage at the noninverting input which is grounded. When the switch is in the left position, the bottom of the $2R$ resistor is held at ground voltage or 0 V by the operation of the op-amp. It is therefore at a virtual ground. The voltage at the mid point of the potential divider, marked X in the circuit, is therefore independent of the position of the switch and in this case the voltage is given by $\frac{V_{ref}}{2}$.

The current into the op-amp I–V converter is therefore the voltage at point X divided by the resistor to the switch, $2R$, which gives $I = \frac{V_X}{2R}$ and the output of the current to voltage converter is this current multiplied by the feedback resistor R_f. In this case V_X is half of the reference voltage V_{ref}, which therefore gives:

$$V_{out} = -\frac{V_{ref}}{2 \times 2R} R_f \quad \text{or} \quad 0$$

depending on the position of the switch.

At the point where V_{ref} is applied, the input resistance of the ladder is $R + R = 2R$ so if we put a copy of this elemental ladder into the circuit, where the right hand $2R$ termination resistor is located, we do not disturb or change the voltages in the circuit. This insertion can be repeated a number of times and the resulting circuit is shown in Figure 54.3.

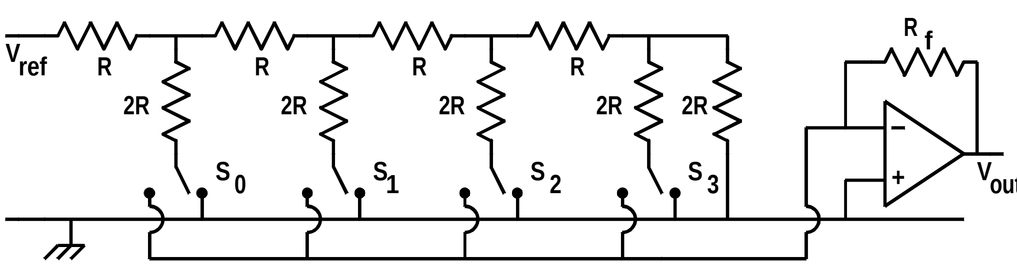

Figure 54.3: R–$2R$ ladder network.

The voltage at the equivalent of point X in the elemental ladder is reduced by a factor of 2 as we progress from left to right along the ladder. For clarity, the diagram only shows the circuit for 4 bits or stages of the ladder but it is easily extended to an 8 bit ladder.

The switches used in the ladder are not mechanical switches but are fabricated on the chip using enhancement mode MOSFETs connected to ground and controlled by the voltages on the relevant wire of the 8 bit data bus as shown in Figure 54.4 (a).

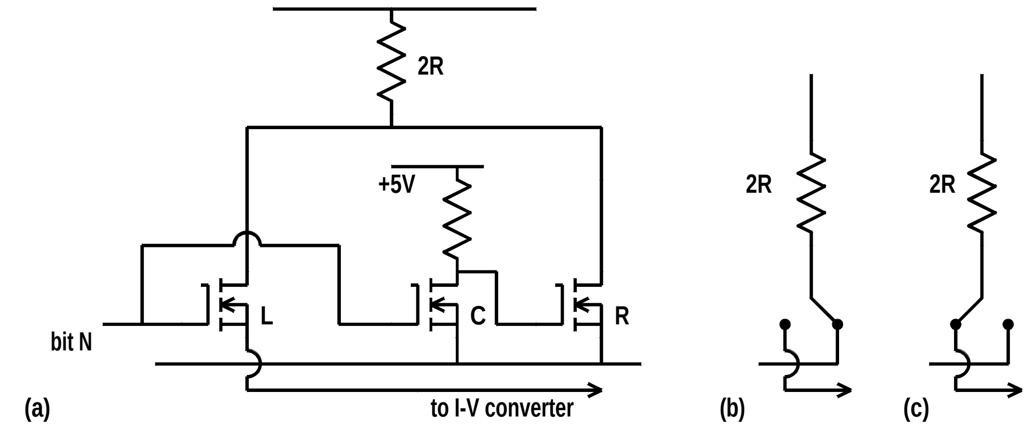

Figure 54.4: FET switches used with R–$2R$ ladder network.

If the signal on the data line for bit N is at 0 V then FET L is OFF. FET C is also OFF so its drain voltage is at +5 V and FET R is ON so that the equivalent switch is as shown in Figure 54.4 (b).

If the signal on the data line for bit N is at +5 V then FET L is ON. FET C is also ON so its drain voltage is at 0 V and FET R is OFF so that the equivalent switch is as shown in Figure 54.4 (c).

The current to voltage circuit in Figure 54.3 sums all of the currents through the $2R$ resistors from each of the voltage tap-off points on the R–$2R$ ladder and gives an output voltage:

$$V_{out} = -R_f \frac{V_{ref}}{4R} \left(S_0 + \frac{S_1}{2} + \frac{S_2}{4} + \frac{S_3}{8} + \dots \right)$$

where S_N is the digital state of the relevant line on the data bus and takes the value 0 or 1.

The advantages of this R–$2R$ ladder network are that:

- Only two values of resistors (or one value if two are used in series) are required to be fabricated on the silicon chip.
- Typical values are 10 kΩ.

- The fabrication can be carried out to the required precision if only one value is required.
- The resistors do not have to be precise values. They only need to be equal valued.

All of these features make this the most convenient DA converter for fabrication as an IC. For high precision it is possible individually to trim the resistors values on the chip by using a focused laser beam to cut out small sections of the resistive track. These high precision DA converters using laser trimmed resistors are more expensive and would only be used in critical applications.

54.1 Problems

In all of these problems you may assume that the resistive ladder is an R–$2R$ network of $10\,\mathrm{k}\Omega$ and $20\,\mathrm{k}\Omega$ resistors, as shown in Figure 54.3, and that the feedback resistor in the I to V converter is $10\,\mathrm{k}\Omega$.

54.1 Calculate the output from an 8 bit DA converter for switch settings 01101010 when the reference voltage is 1 V.

54.2 Calculate the switch settings if an output of 0.63 V is to be obtained from an 8 bit DA with a reference voltage of 4 V.

54.3 What is the smallest increment of output from an 8 bit converter having a reference voltage of 1 V?

54.4 What is the smallest increment of output from a 12 bit converter having a reference of 1 V?