Unit 38 MOSFET and CMOS

- The depletion type MOSFET conducts for a gate to source voltage of zero.
  It is a **normally on** device.
  Drain current drops to zero at $V_{GS(off)}$.
- The enhancement type MOSFET does not conduct for a gate to source voltage of zero.
  It is a **normally off** device.
  The device starts to conduct at threshold voltage $V_{GS(th)}$.
- CMOS devices use complementary p and n channel enhancement type MOSFETs in one integrated circuit of two or more MOSFETs.

MOSFET fabrication. The starting point for MOSFET (Metal Oxide Silicon Field Effect Transistor) fabrication is a lightly doped silicon wafer with a surface layer of silicon dioxide. The photoresist, etch and diffusion processes described in Unit 36 are used to form two heavily doped, isolated regions or wells on the wafer. In the n channel depletion type MOSFET these wells are n-type. An n-type channel is then formed which links the source and drain n^+ wells. (n^+ denotes heavily doped n-type.) In the n channel enhancement type MOSFET this n-type doped channel is not fabricated.

A very thin layer of silicon dioxide is formed over the channel region and a metallized gate region is formed on the silicon dioxide over the channel. A thick silicon dioxide layer is deposited over the device and windows are etched through this silicon dioxide to permit metal contacts to be made to the n^+ source and drain wells and to the gate metallization. It is a fundamental feature of MOSFETs that there is no conducting path between the gate lead and the channel. The gate is isolated by the thin silicon dioxide layer (effectively a glass insulator) which separates it from the channel. This is why you will sometimes see the MOSFET referred to as an IGFET (Insulated Gate Field Effect Transistor).

Since there is an insulating oxide layer between the gate and the channel in the MOSFET, the source, drain and channel can be fabricated as a linear or rectangular structure with the gate overlaying the channel but insulated

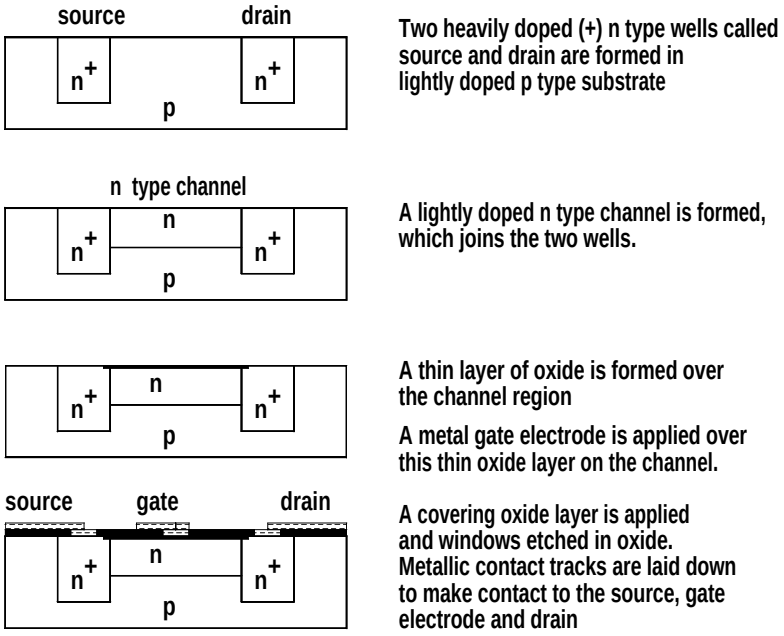

Figure 38.1: Stages in the fabrication of an n channel MOSFET.

from it. The annular structure used in the JFET is no longer necessary in order to prevent a short between the gate and substrate. This means that the fabrication masks for MOSFETs can be rectangular strips, which allows a much simpler fabrication process to be used and which also gives a higher device packing density. This is one of the reasons why the MOSFET technology is so widely used for high density computer chip and memory chip manufacture.

This insulating layer gives the MOSFET its very high input resistance which is in excess of $10^9\,\Omega$. However, this thin silicon dioxide layer is also the weak point in MOSFETs. If the MOSFET is handled without taking precautions to avoid static, the high voltages associated with static (a few thousand volts) can cause a spark discharge to punch through the thin silicon dioxide in the gate region and destroy or shorten the life of the MOSFET.

The depletion mode MOSFET. Depletion mode MOSFET characteristic curves are shown in Figure 38.2 and are similar to those for the JFET except that, because of the insulated gate, it is now permissible to operate the device with either a negative or a positive bias voltage on the gate. The gate voltage at which the drain current is cut off is called the gate-source cutoff voltage, $V_{GS(off)}$ or V_{off}.

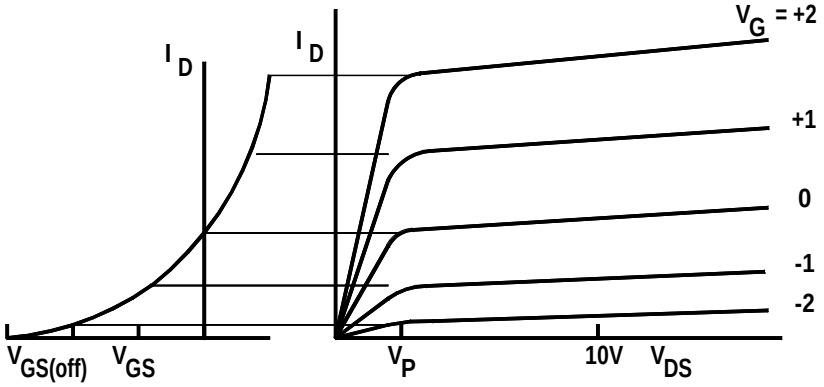

Figure 38.2: n channel depletion mode MOSFET characteristic curves.

If the voltage applied to the gate is negative, the MOSFET operates in depletion mode and the gate electrode voltage repels the channel electrons from the region under the gate electrode, reducing the width of the conducting channel and reducing the drain current. The pinch-off mechanism which we discussed in the case of the JFET also operates whereby increased drain voltage pinches the channel to give a nearly constant drain current.

If the gate voltage is positive, the MOSFET operates in enhancement mode and electrons are attracted into the channel by the positive gate voltage to give increased drain current. There is a second mechanism which can be considered to operate. Holes in the substrate are repelled from under the gate by the positive voltage applied to the gate and this leads to an increase in the number of electrons in the channel region because of the semiconductor equation, $n \times p = n_i^2$ (see Unit 22). If p in $n \times p = n_i^2$ decreases then n must increase.

The main advantage of being able to put voltages of either polarity on the gate is that it is possible to use circuits such as that shown in Figure 38.3 (a) where no reverse bias is applied to the gate but the gate is allowed to vary on either side of zero volts. Figure 38.3 (b) shows the variation of the gate voltage and the resulting variation of the drain current. The fact that a source resistor, R_S, is not needed is not a significant saving in a single circuit but if MOSFETs are used in integrated circuits containing many hundreds of such amplifiers in a single circuit block then the saving can be significant.

Note the circuit symbol used for the depletion mode, n channel MOSFET used in the circuit. The channel is represented by a continuous bar, the gate is isolated from the bar and the fact that the channel is n-type is indicated by the direction of the diode arrow from the substrate to the channel. A p-type channel MOSFET has the diode arrow pointing in the other direction.

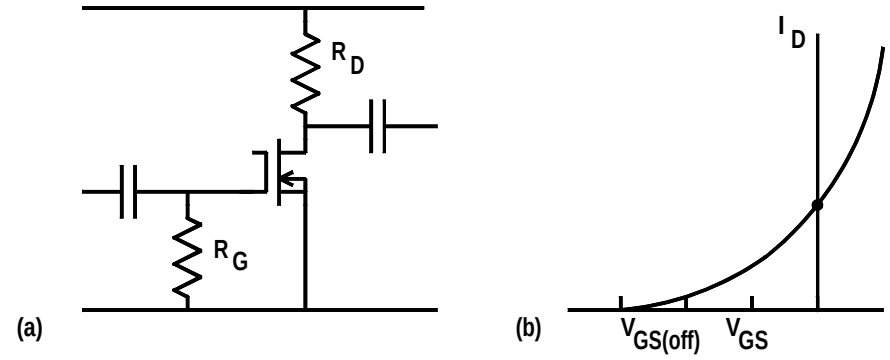

Figure 38.3: Basic MOSFET amplifier circuit and input characteristic.

The enhancement mode MOSFET. The n channel enhancement mode MOSFET is fabricated without a doped n-type channel connecting the n^+ source and drain wells. The application of a large enough positive voltage, called a threshold voltage, $V_{GS(th)}$, to the gate causes an n-type inversion layer to be formed in the p-type region between the source and the drain due to the electrostatic repulsion of the positive gate voltage acting on the p-type carriers. The semiconductor equation, $n \times p = n_i^2$, then gives an increased electron concentration which results in the formation of an n-type channel connecting the source to the drain. The positive gate voltage enhances the conduction in the channel. The characteristic curves for the device are shown in Figure 38.4.

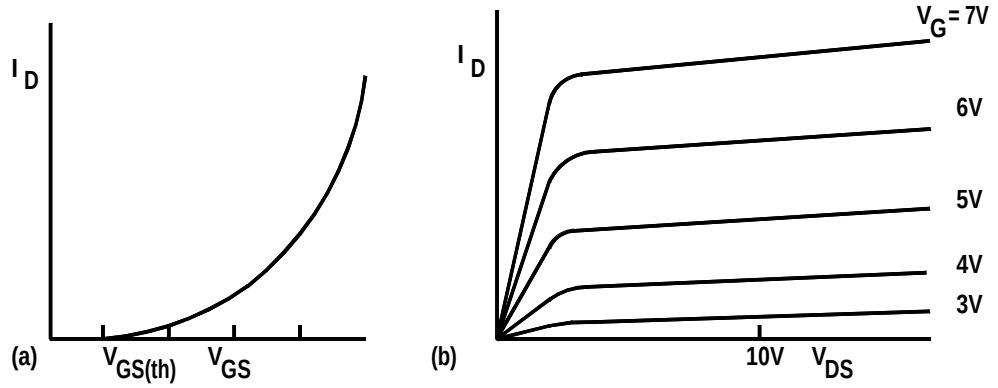

Figure 38.4: n channel enhancement MOSFET characteristics.

It is a fundamental feature of the enhancement type MOSFET that a voltage in excess of the threshold voltage must be applied to the gate before there is any conduction through the device.

Once conduction occurs between the source and drain, the current in the drain in the saturation region is given by the equation:

$$I_D = k(V_{GS} - V_{GS(th)})^2$$

where k is a constant for the particular MOSFET in use.

It is not possible to use the concept of I_{DSS} for an enhancement type MOSFET since there is no current for zero gate to source bias. Another difficulty is that many of the component suppliers' catalogs only quote maximum ratings for the components. It is therefore necessary to have a quick way of determining the MOSFET parameters. The circuit in Figure 38.5 (a) allows the threshold voltage, $V_{GS(th)}$, to be determined since $I_D \approx 0$ and then $V_{GS} = V_{GS(off)}$. In the circuit in Figure 38.5 (b), the drain current is determined from the voltage drop across the drain resistor. This gives an I_D and V_{GS} which can be inserted into the equation for I_D, above, and which will then allow k to be calculated.

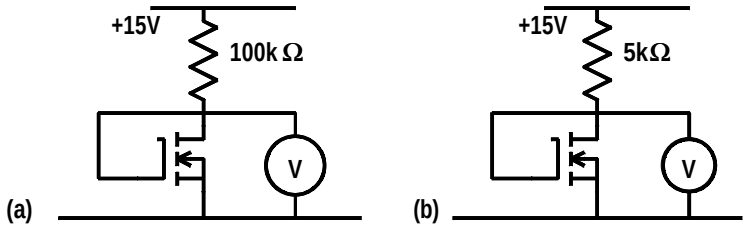

Figure 38.5: Determination of enhancement MOSFET parameters.

Figure 38.6 shows two possible bias configurations for the enhancement type MOSFET. In both circuits, the supply voltage must be greater than the threshold voltage. The circuit in Figure 38.6 (a) has the disadvantage that the gate bias is equal to the supply voltage and this imposes some restrictions on the supply voltage. You should note that the circuit symbol for the enhancement type MOSFET is characterized by an interrupted bar for the channel. The type of channel and the gate are identified by the direction of the diode arrow from the substrate in the same way as in the depletion type MOSFET.

The main advantage of MOSFET devices for analog electronics is the very high input resistance which makes them ideal for input stages of instrumentation devices such as pH meters, multimeters, oscilloscopes, radio receivers etc., which require a high input impedance first stage. Variations of the MOSFET such as the VMOS, the HEXFET, the SIPMOS, in which the channel length is made as short as possible, are used for high current and high frequency operation in applications such as radio transmitters in mobile

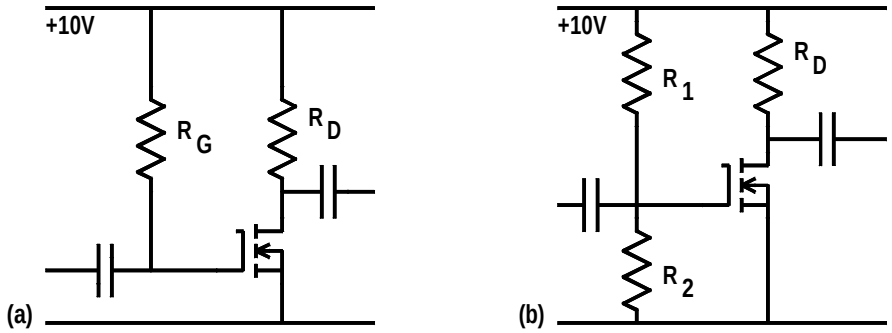

Figure 38.6: Two types of MOSFET bias circuit.

phones, switched mode power supplies and other mobile, portable or battery powered devices.

CMOS. Complementary Metal Oxide Silicon FETS are combinations of p and n channel MOSFETs fabricated side by side on the same wafer. In general the MOSFETs are used as active load type devices where load resistors are replaced by MOSFETs.

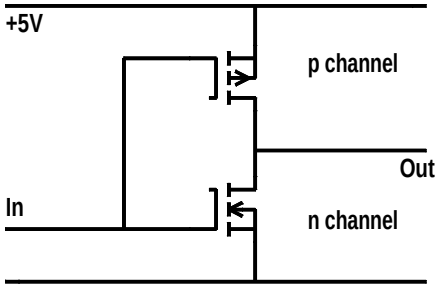

Figure 38.7: CMOS inverter.

A typical circuit configuration is shown in Figure 38.7. A p channel MOSFET is used at the top and an n channel MOSFET is used at the bottom. The two drains are connected together and connected to the output.

Consider the two extreme cases.

If the input voltage to the circuit is at 0 V, then the lower n channel MOSFET gate is below the threshold voltage and the MOSFET is off or nonconducting. However, the gate to source voltage for the upper MOSFET is above the threshold voltage and the upper MOSFET is on and conducting so that the output is connected to the supply voltage.

If the input voltage is at the supply voltage, then the lower MOSFET gate is above the threshold voltage and the lower MOSFET is conducting to give 0 V at the output. The upper MOSFET gate to source voltage is 0 V

and therefore the upper MOSFET gate voltage is below threshold and is off and nonconducting.

Effectively, we have an inverter where 0 V in gives V_{sup} out and V_{sup} in gives 0 V out. This is a circuit in which one of the MOSFETs is always off so that there is no quiescent current which is what makes this type of circuit suitable for use in battery powered devices.

38.1 Example

38.1 The circuit in Figure 38.8 (a) shows an analog switch which uses an enhancement type MOSFET. The input signal can have any value in the range −5 V to +3 V. Calculate the output voltage for a load resistor of 10 kΩ when the control input is at −5 V and when the control input is at +5 V. The threshold voltage for the MOSFET is +2 V.

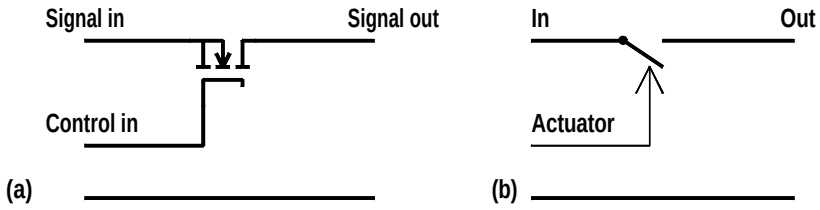

Figure 38.8: MOSFET analog switch.

In this type of analog switch, the control is isolated from the signal which is being switched. The effective switch is shown in Figure 38.8 (b) and is connected between the input and output.

When the control input is at −5 V, the gate to source voltage is in the range from 0 V to −8 V because the source can be at any voltage within the limits −5 V to +3 V. There is therefore no channel formed between the source and the drain and effectively the switch contacts between the input and output are open and the switch is OFF.

When the control input is at +5 V, the gate to source voltage is in the range from +10 V to +2 V for input voltages between −5 V and +3 V. The channel has therefore been formed in the enhancement MOSFET and therefore the resistance between the source and drain is low, typically of the order of 1 kΩ. The input is then connected to the output and effectively the switch is ON. The output voltage will then be close to the input voltage but there will be some reduction in the voltage due to the potential divider action of the source to drain resistance and the 10 kΩ load resistor. In this case the output voltage will be $\frac{10}{11}V_{in}$.

This type of analog switch is available as an integrated circuit (CMOS 4066B type device) which has the feature that the ON resistance is of the order of 50 Ω with the result that the voltage loss in the device is smaller than we have in this example.

38.2 Problems

38.1 An enhancement type MOSFET has a $V_{GS(th)} = +3\,\text{V}$ and also $I_D = 3\,\text{mA}$ when $V_{GS} = +5\,\text{V}$. Sketch the characteristic curves for the device.

38.2 The drain current of an enhancement type MOSFET is given by:

$$I_D = k(V_{GS} - V_{GS(th)})^2$$

Obtain an expression for g_m for the device.

38.3 The test circuits in Figure 38.5 were used to obtain a $V_{GS(th)} = 2.7\,\text{V}$ and an $I_D = 2.3\,\text{mA}$ for a $V_{GS} = 4.2\,\text{V}$. Calculate the value of k in the equation for I_D.

38.4 Calculate the drain current and voltage for the circuit in Figure 38.9. Use the MOSFET from Problem 38.3.

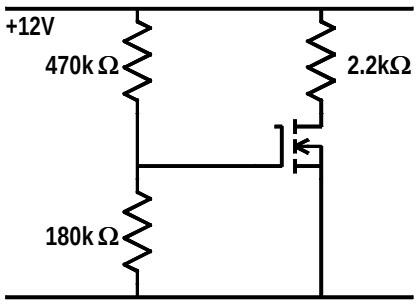

Figure 38.9: Problem 38.4.

38.5 An IRFD110 n channel enhancement type MOSFET is used in an amplifier circuit such as that in Figure 3 8.6 (b). The amplifier is to have a gain of -40. Calculate suitable values for the resistors in the circuit and sketch the circuit.

The IRFD110 device has $V_{GS(th)} = 3\,\text{V}$, $g_m = 0.56\,\text{S}$ and $I_D = 0.22\,\text{A}$ for $V_{GS} = 6\,\text{V}$ and $V_{DS} = 10\,\text{V}$.