Unit 37 JFET amplifiers

- To autobias a JFET amplifier, select: $R_S = \left|\frac{V_{GS(off)}}{I_{DSS}}\right|$
- This gives a gate to source voltage of: $V_{GS} \approx 0.4 \times V_{GS(off)}$
- The drain current is then: $I_D \approx 0.4 \times I_{DSS}$
- The common source small signal gain is: $A_V = -g_m \times R_D$
- Typical small signal gains are of the order of 10.
- Typical input impedances are of the order of 1 MΩ.

If you consult the components catalog of a typical electronic component supplier, you will find that the only readily available parameters for a junction field effect transistor, such as the 2N3819, are I_{DSS}, $V_{GS(off)}$ and g_m together with the maximum voltage and current ratings. A full set of characteristic curves may be available from the component manufacturer but obtaining them can take time. We have to be able to use a JFET even when a full set of characteristic curves is not readily available or without having to reconstruct them from the available data. (See Problem 36.1.)

Another difficulty is that the catalog values for I_{DSS}, $V_{GS(off)}$ and g_m are average values for that JFET type number. A particular JFET, taken out of the storage bin at random, may have parameter values significantly different from the catalog values and still be within the acceptable product specification spread. It is therefore necessary to have a quick method of measuring the parameters for a particular JFET before using it.

The circuit shown in Figure 37.1 (a) shows how the I_{DSS} can be measured directly. Note that the gate is connected to the source to give $V_{GS} = 0\,\text{V}$. The circuit in Figure 37.1 (b) gives a very small value of I_D since the current through the 20 kΩ gives a V_{GS} so close to the cutoff voltage that it can

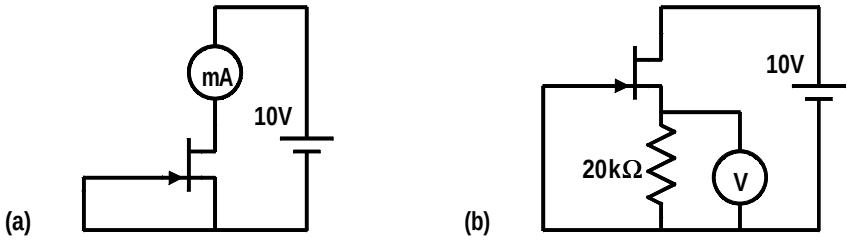

Figure 37.1: Circuits to measure I_{DSS} and $V_{GS(off)}$ for a JFET.

be taken to be equal to the gate-source cutoff voltage. These two simple measurements give I_{DSS} and $V_{GS(off)}$ for the particular JFET in use.

The equation for JFET drain current at any gate to source voltage is:

$$I_D = I_{DSS} \times \left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

Differentiate this to get:

$$g_m = \frac{dI_D}{dV_{GS}} = -2\frac{I_{DSS}}{V_{GS(off)}}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)$$

Note that g_m is positive since both V_{GS} and $V_{GS(off)}$ are negative quantities.

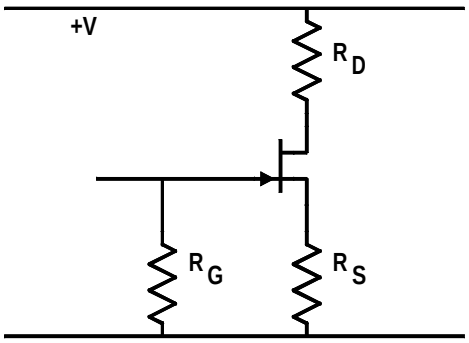

Figure 37.2: JFET amplifier autobias circuit.

Before using a JFET as an amplifier it is necessary to bias the JFET correctly. Consider the simple autobias circuit, shown in Figure 37.2, in which the source current through the JFET also flows through R_S to give a reverse bias of $I_D \times R_S$ between the gate and source. The gate voltage is 0 V because no significant current flows through R_G and through the reverse biased gate to channel junction.

There is a wide range of possible values for R_S which will give a reasonable bias configuration. The most straightforward procedure for selecting the value of R_S is to use:

$$R_S = \frac{V_{GS(off)}}{I_{DSS}}$$

This causes the bias point to be at the intersection of the line for R_S and the curve for V_{GS} shown in Figure 37.3.

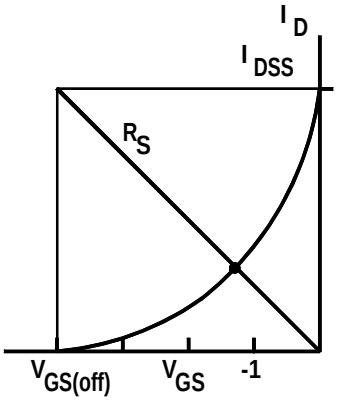

Figure 37.3: Method of selecting R_S.

We then have $V_{GS} = I_D \times R_S = I_D \times \frac{V_{GS(off)}}{I_{DSS}}$ which gives:

$$\frac{V_{GS}}{V_{GS(off)}} = \frac{I_D}{I_{DSS}}$$

But we also have the equation for I_D for the JFET:

$$\frac{I_D}{I_{DSS}} = \left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

Substitute $\frac{V_{GS}}{V_{GS(off)}}$ for $\frac{I_D}{I_{DSS}}$ in this equation to get an equation of the form $x = (1-x)^2$ which has solutions $x \approx 2.6$ and $x \approx 0.4$.

Take the only physically possible solution, $x \approx 0.4$, to get:

$$\frac{V_{GS}}{V_{GS(off)}} = \frac{I_D}{I_{DSS}} = 0.4$$

This method of biasing the JFET then gives a drain current of:

$$I_D = 0.4 \times I_{DSS}$$

By following this procedure, a reasonable bias point is obtained for the simple autobias circuit. However, you should remember that this is just one

bias point out of a range of possible bias points so you will find other values used in circuits.

The next step in the design of a JFET amplifier is to select the value for the drain resistance, R_D.

If a small signal is coupled to the gate through a capacitance, the operating point is momentarily displaced from the DC bias point. The source voltage can be maintained constant by the use of a capacitor connected across the source resistance. This configuration is shown in Figure 37.5.

The mutual conductance, g_m, relates the change in drain current to a change in the gate voltage:

$$g_m = \frac{dI_D}{dV_{GS}} = \frac{i_d}{v_g}$$

The drain resistor relates the change in drain current to the change in the output voltage:

$$v_d = -R_D \times i_d$$

Combine these two relationships to get the small signal voltage gain:

$$A_V = \frac{v_{out}}{v_{in}} = \frac{v_d}{v_g} = \frac{-R_D \times i_d}{\frac{i_d}{g_m}} = -g_m R_D$$

If the required gain, A_V, is specified, the value for R_D is calculated from:

$$R_D = \frac{-A_V}{g_m}$$

The load line can now be drawn as R_D on the characteristic curve shown in Figure 37.4. It is necessary that this load line intersects the horizontal

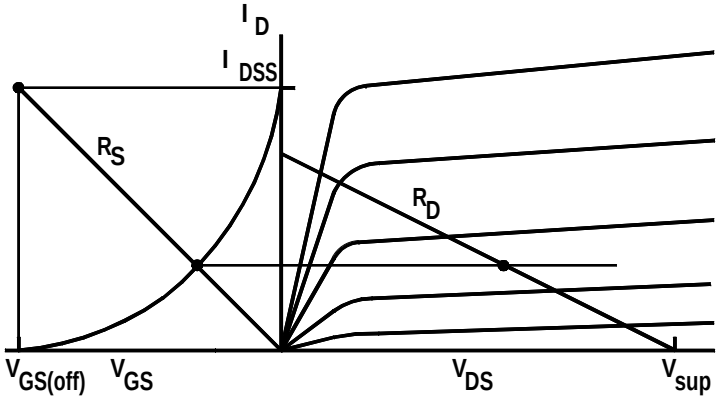

Figure 37.4: Identification of required load line.

line corresponding to $I_D = 0.4 \times I_{DSS}$ so we then obtain a minimum required value for the power supply voltage. Typically we require that the load line intersects the I_D axis at a point well above $0.4 \times I_{DSS}$. It can be seen from Figure 37.4 that if the same value of R_D were to be used with a smaller supply voltage, the load line and the horizontal line for I_D would not intersect within the range of the characteristic curves.

If the load line of slope R_D is drawn through the point $2 \times 0.4 I_{DSS} = 0.8 I_{DSS}$ on the I_D axis then there is enough available voltage across R_D to allow the drain voltage to swing equal amounts in the + and − directions. This criterion then allows an optimum supply voltage to be selected as:

$$V_{sup} = 0.8 \times I_{DSS} \times R_D$$

Since g_m is of the order of $2000\,\mu$S and R_D is typically of the order of $5\,\text{k}\Omega$, small signal gains of the order of $g_m \times R_D = 10$ are expected for JFET amplifiers. This is much lower than the gains of approximately 200 which are obtained with bipolar transistor amplifiers. However, the JFET amplifier has the advantage that the input impedance is much higher and is set by the resistance connected to the gate.

37.1 Example

37.1 Calculate the component values and supply voltage for the circuit in Figure 37.5, so as to obtain a small signal voltage amplification, $A_V = -6$ and an input impedance of $500\,\text{k}\Omega$.
The JFET used in the circuit has the following parameter values:
$g_m = 2500\,\mu$S, $V_{GS(off)} = 2.5\,$V and $I_{DSS} = 7.5\,$mA.
(In this example, the calculated component values have been inserted in the diagram.)

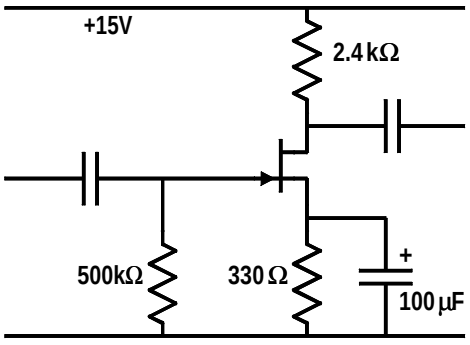

Figure 37.5: Circuit for Example 37.1.

Since R_{in} is to be 500 kΩ and the input gate resistance of the JFET is $\gg 1\,\mathrm{M}\Omega$, we pick $R_G = 500\,\mathrm{k}\Omega$ to give the required input impedance for the amplifier.

We obtain a reasonable value for R_S by setting:

$$R_S = \frac{V_{GS(off)}}{I_{DSS}} = \frac{2.5\,\mathrm{V}}{7.5\,\mathrm{mA}} = 330\,\Omega$$

If we draw a simplified set of generic JFET characteristics as shown in Figure 37.6, we can see the approximate position of the drain current.

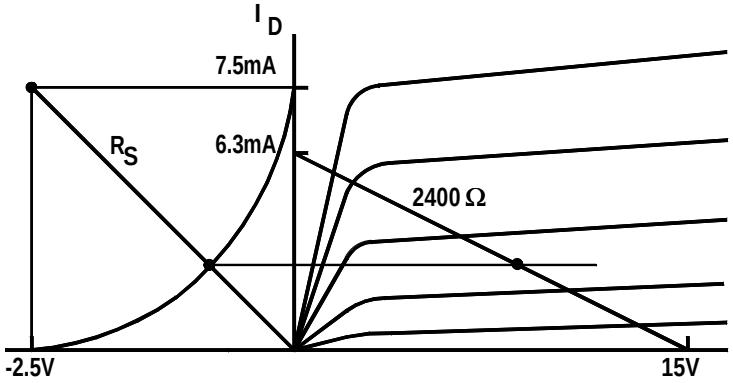

Figure 37.6: Load line for Example 37.1.

We need a small signal gain of −6. Therefore:

$$A_V = -6 = -g_m \times R_D = -2500 \times 10^{-6} \times R_D$$

This gives $R_D = \frac{6}{2500 \times 10^{-6}} = 2400\,\Omega = 2.4\,\mathrm{k}\Omega$

This load line is sketched in Figure 37.6 (note that the voltage drop across R_S has been neglected). The line for the drain current of $0.4 \times 7.5\,\mathrm{mA} = 3\,\mathrm{mA}$ from the R_S selection calculation must intersect the load line for R_D in the central region of the JFET characteristics. It can be seen that a supply voltage of 15 V gives a reasonable intersection point.

37.2 Problems

(Unless otherwise stated, the parameter values for the JFETs used in these problems are: $g_m = 2000\,\mu\mathrm{S}$, $V_{GS(off)} = -4\,\mathrm{V}$ and $I_{DSS} = 9\,\mathrm{mA}$).

37.1 If the power supply voltage in Example 37.1 is reduced from +15 V to +6 V, will the amplifier still be biased correctly?

37.2 A JFET is selected at random from the storage bin. How would the I_{DSS} and the $V_{GS(off)}$ for the JFET be measured?

37.3 If the JFET in the circuit in Figure 37.5 is replaced and the new value of the source voltage is found to be $V_S = 1.4\,\text{V}$, calculate the new drain current and the new drain voltage.

37.4 Calculate the component values and supply voltage for the circuit in Figure 37.7 which give a small signal voltage amplification, $A_V = -7$, and an input impedance $R_{in} = 1\,\text{M}\Omega$.

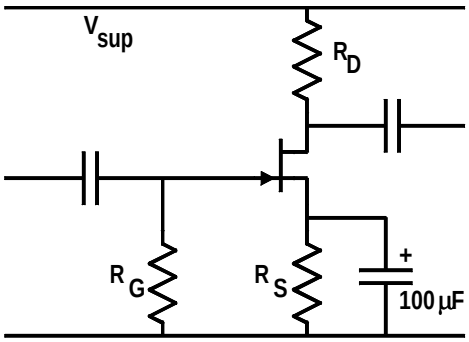

Figure 37.7: Problem 37.4.

37.5 Sketch the voltage waveforms which you would observe with an oscilloscope connected to the input, the gate, the source, the drain and the output in the circuit of Problem 37.4 when a 1 kHz sinusoidal signal of amplitude 70 mV is applied to the amplifier input.

37.6 Calculate suitable values for the resistors for the source follower circuit shown in Figure 37.8. What would be a reasonable value for the supply voltage?

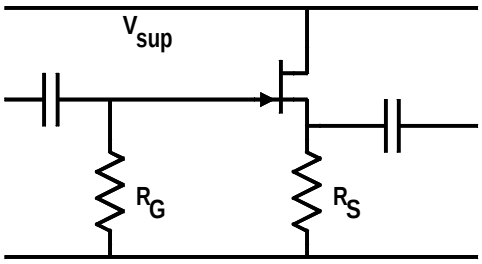

Figure 37.8: Problem 37.7.

37.7 What is the time constant for the filter formed by the R_S and the $100\,\mu$F in the circuit of Problem 37.4?
What is the corner frequency corresponding to this time constant?
Will the design voltage gain of -7 be obtained for frequencies below this corner frequency?

37.8 Calculate suitable values for the source resistor, R_S, in the circuit shown in Figure 37.9. (Hint: Calculate the I_D as in Problem 37.4 and then increase the value of R_S to allow for the increased voltage corresponding to the voltage at the mid point of the potential divider.)

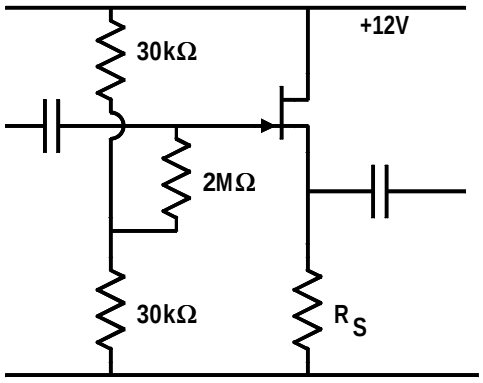

Figure 37.9: Problem 37.8.

37.9 Calculate the drain current for the circuit in Figure 37.10. Calculate the source, drain and gate voltages.

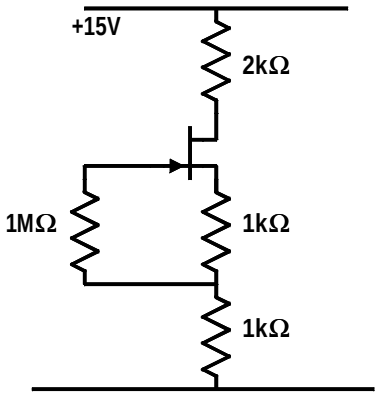

Figure 37.10: Problem 37.9.