# Unit 36 Junction field effect transistors

In the semiconductor fabrication process:

- Silicon dioxide is an insulator.
- Silicon dioxide can be formed on silicon substrates.
- Etchant preferentially dissolves silicon dioxide.
- Photoresist protects silicon dioxide from being etched.
- Silicon dioxide prevents dopants from reaching the silicon.

In JFET operation:

- Increasing drain to source voltage gives increased drain current.
- Increasing drain voltage pinches off the conduction channel and reduces the drain current.
- These two processes partially cancel out.

A JFET is specified by three main parameters:

$V_{GS(off)}$ = Gate to source cutoff voltage

$I_{DSS}$ = Drain saturation current for zero gate to source voltage

$g_m = \dfrac{dI_D}{dV_{GS}}$ = Mutual conductance

**Fabrication processes.** Before examining how a junction field effect transistor operates, we consider some of the unit operations which are used in the fabrication process and see how these operations are combined in sequences in the fabrication of bipolar transistors and FETs.

A silicon wafer is a 0.5 mm thick, 100 mm, 150 mm or 200 mm diameter disk of silicon sliced, parallel to a crystal plane, from a large, raw crystal or boule of high purity, lightly doped p-type or n-type silicon. This wafer is the substrate on which transistors, FETs and integrated circuits are fabricated.

The surface layer of the silicon wafer is usually coated with a thin native oxide layer of $SiO_2$ about 0.1 nm thick. The thickness of this layer of silicon dioxide can be increased by an oxidizing process in which the wafer is heated to a temperature of the order of 1000 K in an atmosphere of steam and oxygen which results in the oxidation of the surface layer of the silicon wafer to silicon dioxide. Other methods of oxidation include electrochemical anodization and plasma reaction.

Instead of oxidizing the silicon of the wafer, a silicon dioxide layer can also be formed on the wafer by a chemical vapour deposition process in which silane ($SiH_4$) gas is reacted with oxygen gas to leave a deposit of silicon dioxide on the wafer surface. This method is used for forming thicker layers of silicon dioxide.

The silicon dioxide, which is essentially a layer of glass, can be dissolved by etching the wafer in hydrogen fluoride (HF). The HF does not dissolve the silicon.

A photoresist is an organic material that can be coated or spun on to the wafer surface to give a layer about a micron thick. When a negative type photoresist is exposed to ultraviolet light, it polymerizes and hardens. In the developing process, unexposed, unpolymerized photoresist is dissolved and removed. The exposure of the photoresist coated wafer is carried out using a photomask which is a patterned layer of metal on a glass substrate. The UV light passes through the clear areas and exposes the photoresist. The UV light does not pass through the metallized regions of the photomask. After the development process, a hardened resist pattern coats the wafer with a pattern which is the negative of the metal pattern on the mask.

In the next stage of the process the oxide layer in the regions not protected by hardened photoresist is etched away either by immersing the wafer in HF or by use of a plasma etcher. This forms windows in the oxide in the same pattern as the original metal pattern on the mask. When the process is completed the remaining photoresist can then be removed by a plasma ashing process or by a wet chemical process.

The wafer is then placed in a furnace in an atmosphere of either p-type (boron) or n-type (phosphorous) dopant containing gas. The dopant enters the silicon wafer through the windows in the oxide and diffuses down into the wafer. The wafer is protected from the dopant gas in the other regions by the oxide. The sequence of operations is illustrated in Figure 36.1.

If the remaining parts of the oxide layer are etched away, a new oxide layer can be grown on the wafer and the process can be repeated with a different mask pattern and multiple structured layers can be formed in the top layers of the silicon wafer. Metal layers and layers of polysilicon can be evaporated or deposited onto the wafer and etched in patterns in exactly the same way

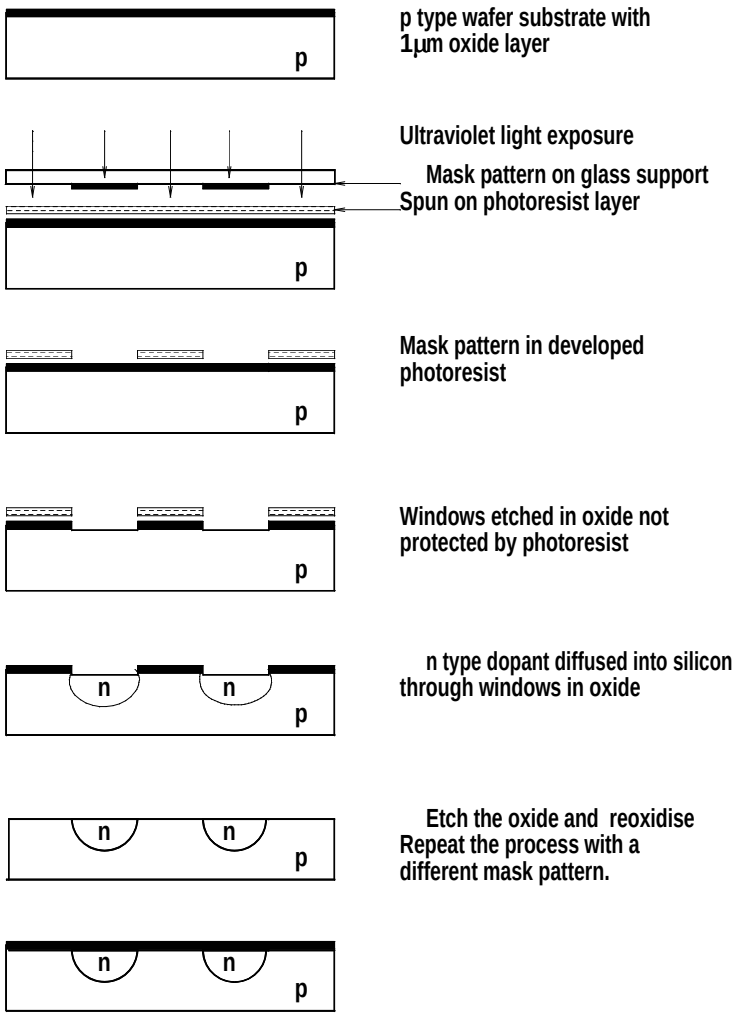


Figure 36.1: Photolithography using a negative photoresist.

as the silicon but using other etchants besides HF. Connections can be made to specific doped regions of the pattern and the connecting tracks can cross each other if silicon dioxide is used as an insulating layer between the tracks. Capacitors can be formed on the the wafer by placing an oxide layer between two metallic layers. If the dopant concentrations are tightly controlled and the n-type or p-type tracks are long then it is also possible to form resistors on the wafer.

Since the mask can contain multiple copies of the same small mask pattern, it is possible to form many thousands of individual transistors or FETs or many hundreds of integrated circuits on a single wafer. At the end of the process, the wafer is scribed and diced and the individual devices can then be

separated, tested, packaged and sold. Since the tracks in the masked patterns can be as small as microns it is important that dust particles, which might give unwanted additional masking, be kept away from the process. This is the reason why the process is carried out in superclean rooms by operators wearing dust free suits. Even with all these precautions, the typical yield, which is of the order of 99% for single transistor manufacture, can drop to 50% for complex integrated circuits such as microprocessor chips or memory chips containing up to a million transistors in a single integrated circuit. Failure of a single transistor of the thousands of transistors in an IC causes the whole IC to be failed at the inspection stage.

**Bipolar transistors.** We have already examined the operation of npn and pnp bipolar transistors. The fabrication of these transistors can, in principle, be carried out using two masks for the diffusion stages with the masks consisting of a simple metal circle pattern. The diameter of the metal is smaller on the second mask. The result of masking, etching and doping an n-type substrate with p-type and then n-type gives the planar structure shown in Figure 36.2 which is an npn transistor. Note that the emitter region started out as n-type substrate, it was then doped p-type during the base region formation and was turned back to n-type by further doping during the emitter region formation.

The connections can be made using thin gold wire welded to metal pads on the base and emitter and to the lead-out wires in the packaging can. The collector, which is the substrate, is often bonded to the metal of the can which then forms the third connection. This is why many transistors have the can connected to the collector. When the collector is bonded to the can, the heat sinking of the silicon transistor is improved since there is good thermal contact between the silicon and the metal can. If there is significant power dissipation in the transistor, the can is often mounted on a heat sink with radiating fins to keep it cool. It can also be seen from Figures 36.2 and 36.3 that the model of an npn bar shaped transistor, with connections at the side, which we used at the beginning of Unit 30, really corresponds to a narrow vertical section of a much wider and flatter structure.

In the microphotograph shown in Figure 36.3, the top of the metal can of a BC109 transistor has been cut off and the silicon chip, the doped areas and the connecting wires are shown. The chip has dimensions about $0.5\,\text{mm} \times 0.5\,\text{mm}$. The small diameter of the wires should be noted. If too large a current is passed through the transistor the connecting wires of small signal transistors tend to heat and fuse giving an open circuit on the lead. This is why simple tests for diode action can usually verify the functioning of signal transistors. The leads of power transistors are usually heavier and can last for long enough for the silicon to overheat and change the performance

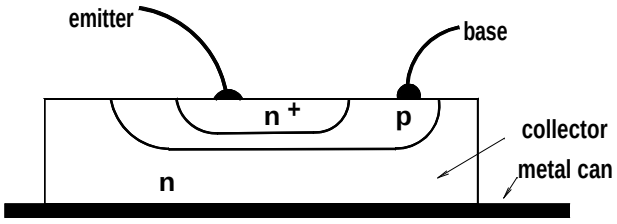


Figure 36.2: Cross section of an npn transistor.

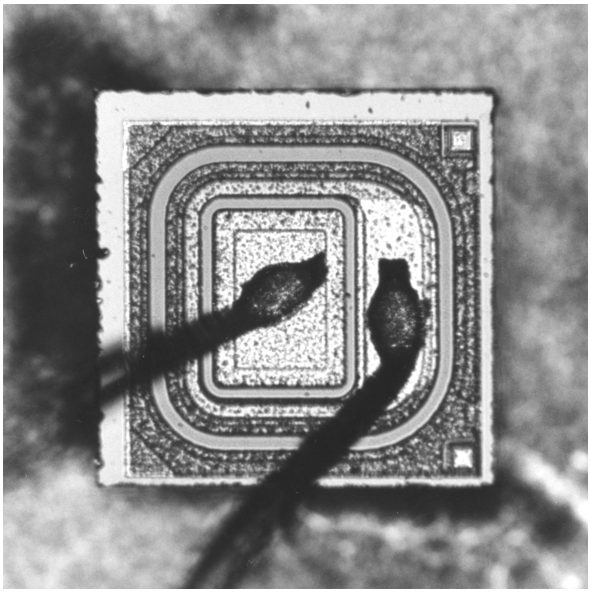

Figure 36.3: Microphotograph of a BC109 transistor.

of the transistors. As a result, more complex checking procedures may be necessary for suspect power transistors in a circuit since they may degrade rather than fail catastrophically.

**Junction field effect transistors.** The unit processes involved in the manufacture of JFETs are the same as those involved in the manufacture of bipolar transistors. The processes are compatible and it is possible to manufacture JFETs and bipolar transistors on the same wafer in integrated circuits. However, a different arrangement of masks is used to give a different geometry for JFETs.

A top view of an n channel JFET is shown in Figure 36.4. The conduction path between the drain and source is along the n channel in the n-type epilayer between the gate and the p-type substrate as shown in the section view of the JFET. If the annular structure shown in Figure 36.4 is

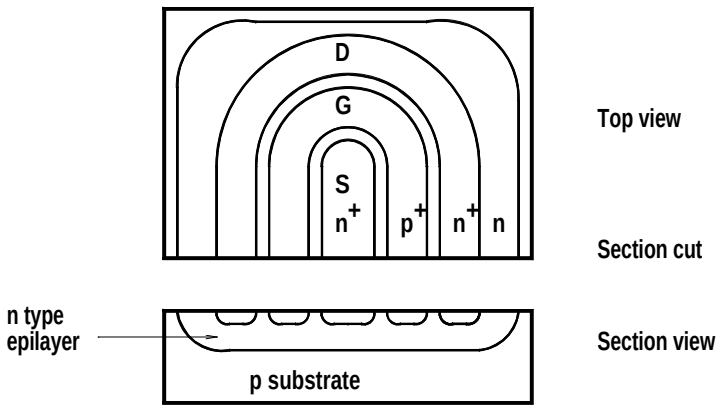


Figure 36.4: Structure of an n channel JFET.

used, it is then possible to fabricate JFETs and not have the gate connected to the substrate. This is an advantage because it allows a metal can encapsulation to be used without the gate being connected to the can. Use of a plastic encapsulation allows this problem to be avoided. The annular structure also allows a number of JFETs to be fabricated on one chip without all of the gates being shorted together so that JFETs can then be combined in integrated circuits on one chip.

The essential difference between the bipolar transistor and the JFET is that the current flows perpendicularly through the thin base region in the bipolar transistor but along the channel in the case of the JFET.

In the fabrication of JFETs, the starting point is a p-type substrate on which an n-type circular region is formed. The central heavily doped n-type source region and outer drain annulus are formed next. Then the heavily doped p-type gate annulus is formed between the drain and source. The n-type channel extends under this gate region and above the p-type substrate. In analyzing the operation of this n channel JFET, we consider a radial section through the device, shown schematically in Figure 36.5.

The depletion layer associated with the heavily doped p-type gate region extends into the channel. As the reverse bias applied to the gate region increases, the channel thickness is constricted. Therefore the application of reverse bias voltage to the gate controls the current flowing in the channel between the drain and source. The JFET is then a voltage controlled device whereas the bipolar transistor is a current controlled device.

In many JFETs, the p-type gate is connected to the p-type substrate and the channel is constricted between the gate and the substrate with a depletion layer above and below.

If this were the full story, the structure would simply behave as a resistor

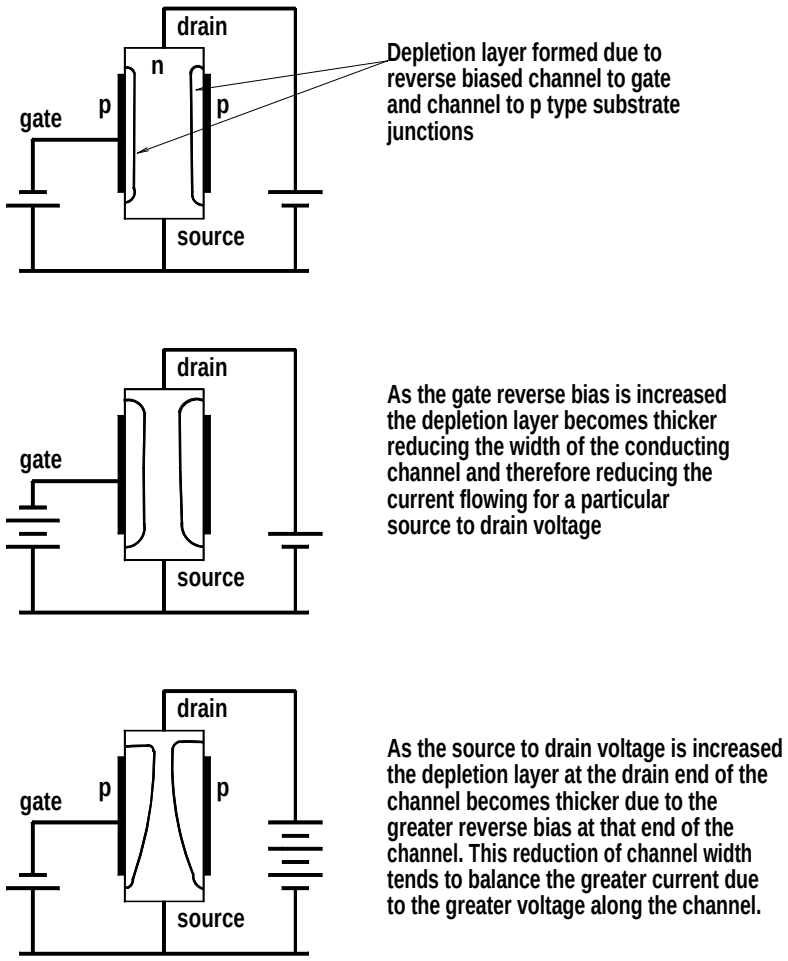


Figure 36.5: Mechanism of operation of a JFET.

between the drain and source having a resistance value determined by the voltage applied to the gate.

However, another mechanism also operates. For voltages greater than what is called the pinch-off voltage, $V_P$, applied between the drain and the source, the increased reverse bias between the upper end of the gate and the drain gives a thicker depletion layer at the top of the channel. This is shown in Figure 36.5. Thus the increased drain voltage, besides driving more current through the channel, also causes a reduction of the channel width which tends to counteract the increased current which would otherwise flow between the drain and the source. Therefore if the gate voltage is kept constant and the drain to source voltage is increased, it is found that the drain current initially

increases in proportion to the drain to source voltage but that it then levels off so that the drain current is nearly independent of the drain to source voltage. The characteristic which results from this pinch-off effect is shown in Figure 36.6.

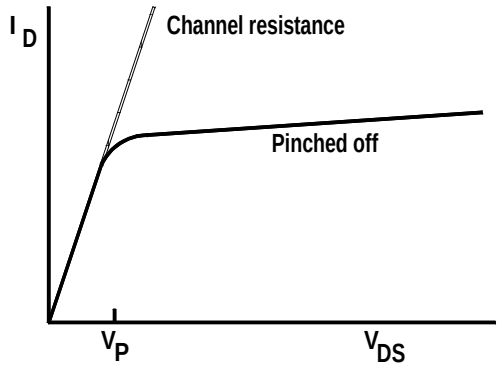


Figure 36.6: Effect of the pinch-off mechanism.

In order to characterize a JFET, a circuit such as that shown in Figure 36.7 is used. This circuit shows an n channel JFET such as a 2N3819 device. The diode arrow on the gate of the JFET symbol indicates the direction of the pn junction diode between gate and channel. The diode arrow for a p channel JFET points in the opposite direction.

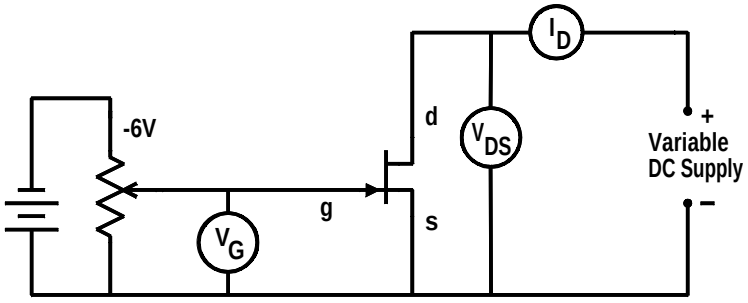


Figure 36.7: Circuit for measuring JFET characteristics.

This circuit allows us to apply a negative voltage between 0 V and $-6$ V to the gate of the JFET, measured with reference to the source. Since the gate to channel is a reverse biased diode there will be no significant current in the gate lead. The circuit also allows us to measure simultaneously the drain to source voltage and the drain current.

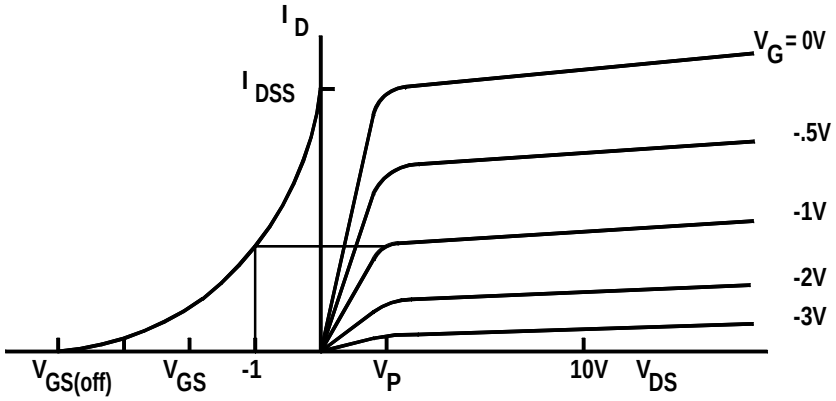


Figure 36.8: JFET characteristics.

Figure 36.8 shows the characteristic curves which result from these measurements. In the right hand set of curves, the drain current is plotted as a function of the drain to source voltage for various constant values of the gate to source voltage. The general shape is a rising region followed by a saturated region in which the current is pinched off. For a gate to source voltage of 0 V, the drain current is a maximum and this value of the drain current is called $I_{DSS}$, the drain saturation current for a gate voltage of 0 V. This saturation occurs for a drain to source voltage, $V_{DS} = V_P$, where $V_P$ is the pinch-off voltage.

In the left hand curve, we plot the drain saturation current for the particular value of the gate to source voltage as a function of the gate to source voltage. The gate to source voltage at which the drain current drops to 0 mA is called the gate-source cutoff voltage, $V_{GS(off)}$.

From a theoretical analysis of the physics of JFETs, which we will not pursue in this text, it is found that the $I_D$ at a particular value of $V_{GS}$ is given by:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

which is the theoretical equation for the curve of $I_D$ versus $V_{GS}$ in the left hand characteristic curve in Figure 36.8. The slope of this curve is the mutual conductance, $g_m$, for the JFET. It can be seen that this is not a constant but depends on the operating point. The data sheets usually quote a value of $g_m$ obtained at some typical JFET operating value. The quoted value for $g_m$ for the 2N3819 JFET is $g_m = 2000\,\mu$S (microsiemens) at $V_{DS} = 5$ V. The siemen is the unit of conductance and has units of $\frac{\text{Amps}}{\text{Volts}}$.

## 36.1 Example

36.1 If $I_{DSS} = 7.5\,\text{mA}$ and $V_{GS(off)} = -3.7\,\text{V}$ for the JFET characteristics plotted in Figure 36.8, calculate the value of $I_D$ when $V_{GS} = -1\,\text{V}$.

$$\begin{aligned} I_D &= 7.5 \times \left(1 - \frac{-1}{-3.7}\right)^2 \text{ mA} \\ &= 7.5 \times (1 - 0.27)^2 \text{ mA} \\ &= 3.99\,\text{mA} \end{aligned}$$

## 36.2 Problems

36.1 The following values were quoted in the data sheet for an n channel JFET:

$$g_m = 2700\,\mu\text{S}, \quad V_{GS(off)} = -4.5\,\text{V} \quad \text{and} \quad I_{DSS} = 7.0\,\text{mA}$$

Reconstruct the characteristic curves for this JFET from this set of values. (See Figure 36.8.)

36.2 If $I_{DSS} = 9.3\,\text{mA}$ and $V_{GS(off)} = -3.7\,\text{V}$ for a JFET having the characteristic shown in Figure 36.8 calculate the value of $g_m$ at $V_{DS} = 10\,\text{V}$ and $V_{GS} = -2\,\text{V}$.

36.3 Draw up a set of masks suitable for use in fabricating the BC109 transistor shown in Figure 36.3. Use negative photoresist.

36.4 What changes would be necessary if positive photoresist was used in Problem 36.3?

36.5 Modify the circuit of Figure 36.7 so that the characteristics of a p-channel JFET can be measured.