DUBLIN CITY UNIVERSITY

May 2000

COURSE:	APPLIED PHYSICS PHYSICS with a LANGUAGE
YEAR:	2
SEMESTER	1
EXAMINATION:	Electronics 2; PS206
EXAMINER:	Dr B. Lawless
DURATION:	2 hours
INSTRUCTIONS:	Answer 5 parts of Question 1 (50 %) and 2 other questions (25 % each)
	Hand up page 5 of this question book with your answer.
	Do not turn over this page until instructed to do so.

Question 1. Answer five parts of this question.

(a) Explain the following:

i. What is meant by "current sinking" as it applies to TTL devices?

ii. How does the use of Schottky diodes speed up the operation of TTL devices?

iii. Why does the use of transistors in differential mode gives fast circuit operation in ECL devices?

(b) Write down the sequence of numbers from 0 to 20 in

i. Decimal

ii. Binary

iii. Hexadecimal

iv. Gray code

(c) Explain the meaning of

i. Weighted codes

ii. Nonweighted codes

iii. Cyclic codes

iv. Reflective codes

(d) Draw the logic gate circuit diagram for this Boolean expression

$$Q = \overline{A}.B + \overline{B}.C + \overline{C}.A$$

(e) Draw the logic gate diagram represented by this minterm list

$$Q = f(A, B, C, D) = \Sigma m(0, 2, 5, 12)$$

(f) Draw the logic gate circuit diagram for an RS flip flip constructed from NOR gates and explain the operation of the circuit.

(g) Explain how parity checking is used to detect errors. Explain the difference between error detection and error correction.

(h) Prove De Morgan's theorem.
Give a circuit equivalent of:

$$\overline{A + B} = \overline{A}.\overline{B}$$

Question 2. The truth table for a particular logic system, having a single output Q, is shown below.

(a) Derive the minterm and maxterm lists for the system.

(b) Draw the Karnaugh map for the system and obtain a simplified Boolean expression for the system.

(c) Derive a Sum of Products Boolean expression for the system and draw the Sum of Products circuit (AND/OR).

(d) Derive a Product of Sums expression for the system and draw the Product of Sums circuit (OR/AND).

A	B	C	D	Q
0	0	0	0	1
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

Question 2.

Question 3. Explain how JK flip flops can be used to implement a four bit binary counter. What feature of JK flip flops permits the flip flops to be used to construct counters?
Explain how this binary counter can be modified to implement a Base 10 counter.
Give a table showing the four outputs from the counter as a function of the count sequence.

Question 4. What is meant by "The Canonical Form" of an expression?
Use the identity $\overline{X} = 1 \oplus X$ to convert the expression

$$Q = f(A, B, C, D) = A.B.\overline{C}.\overline{D} + \overline{A}.B.C.\overline{D} + A.\overline{B}.C.D$$

into Reed-Muller Canonical form. Draw the circuit which implements the Reed-Muller expression.

Question 5. Explain the operation of the R-2R ladder network used in the D/A converter shown in Figure 1.

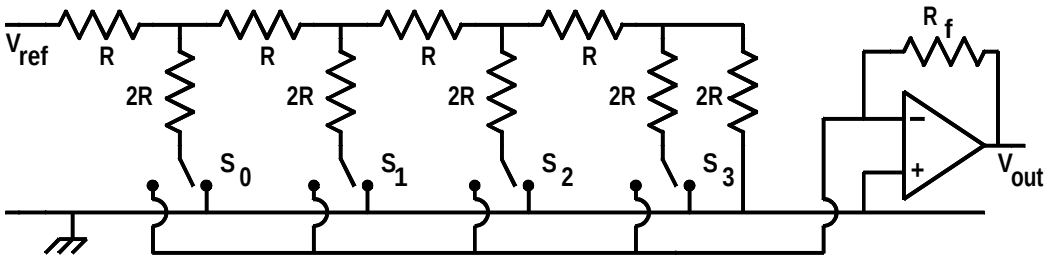

Figure 1: Question 5

Show how this D/A converter can be used to implement an A/D Feedback converter. Discuss the algorithms which are used to control the operation of these feedback A/D converters.

Question 6. Use the table below to minimize the expression specified by the minterm list:

$f(A, B, C, D, E, F, G) = \Sigma m(12, 19, 21, 29, 50, 44, 83, 93, 122) + d(25, 37, 45, 95, 114)$

Verify your result by carrying out the minimization indicated by the table. You should return this page, with the table suitably marked, as part of your answer.

Write your name here .....

0	16	48	32	96	112	80	64
1	17	49	33	97	113	81	65
3	19	51	35	99	115	83	67
2	18	50	34	98	114	82	66
6	22	54	38	102	118	86	70
7	23	55	39	103	119	87	71
5	21	53	37	101	117	85	69
4	20	52	36	100	116	84	68
12	28	60	44	108	124	92	76
13	29	61	45	109	125	93	77
15	31	63	47	111	127	95	79
14	30	62	46	110	126	94	78
10	26	58	42	106	122	90	74
11	27	59	43	107	123	91	75
9	25	57	41	105	121	89	73
8	24	56	40	104	120	88	72

Table for Question 6