Summer 2004

COURSE:	APPLIED PHYSICS PHYSICS with a LANGUAGE Physics Exchange
YEAR:	2
SEMESTER	2
EXAMINATION:	PS206: Electronics 2
EXAMINER:	Dr B. Lawless Ph 7005300
DURATION:	2 hours
INSTRUCTIONS:	Answer 5 parts of Question 1 (50 %) and 2 other questions (25 % each) Hand up page 4 of this question book with your answer.
	Do not turn over this page until instructed to do so.

Question 1. Answer five parts of this question.

(a) Explain the operation of the CMOS NAND gate circuit shown in Figure 1.

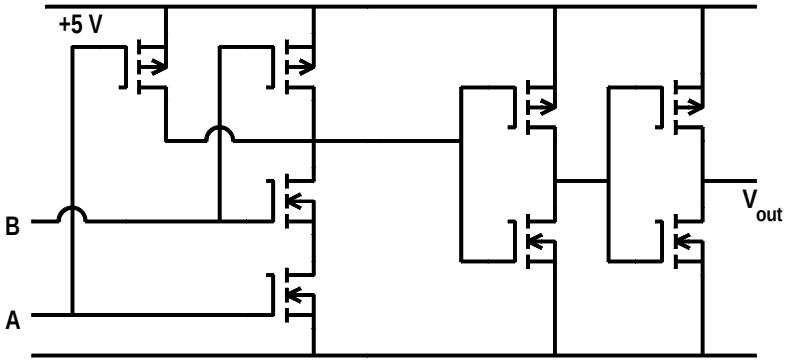

Figure 1: Question 1(a)

(b) Carry out the following conversions and explain the method in each case.

i. Convert 904097_D to Hexadecimal.

ii. Convert $425D4_H$ to Decimal.

iii. Convert $1B6_H$ to Binary.

iv. Convert 61_D to Gray code.

v. Calculate the negative of 0532_H.

(c) Obtain the Boolean expression which corresponds to the circuit shown in Figure 2.

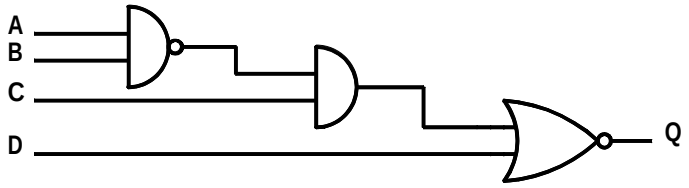

Figure 2: Question 1(c)

(d) Draw a circuit which implements the truth table shown below. Draw the Karnaugh map and use the map to obtain a simplified circuit.

A	B	C	D	Q
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	1
1	1	1	1	1

Truth Table for Question 1 (d).

(e) Obtain the Canonical Sum of Products form for the Boolean expression shown below.

$$Q = A.B.\overline{C} + \overline{A}.B.\overline{C} + \overline{B}.C.D$$

(f) Obtain the Boolean expression for the following minterm list.

$$Q = \Sigma m(1, 3, 8, 10, 15, 16, 23, 29)$$

(g) Obtain the circuit which is equivalent to the circuit shown below in Figure 3 and which uses only NAND gates.

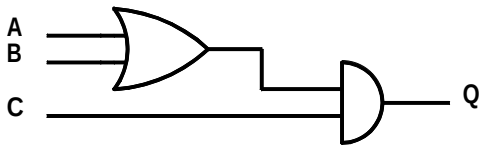

Figure 3: Question 1(g)

(h) Draw the circuit which implements the Boolean expression

$$Q = (A.\overline{B}) \oplus (\overline{C} + D)$$

Question 2. Give an account of the operation of the $\overline{R}\,\overline{S}$ Flip Flop.
Why is the term "Flip Flop" used to describe the circuit?
Why are three of the four states of the circuit stable?
Explain the instabilities associated with the remaining fourth state of the circuit.
Explain how the modifications of using a using an inverter to feed signals to the $\overline{R}$ and $\overline{S}$ inputs together with the use of a clock or gate enables the instabilities to be avoided in the Type D Flip Flop.
Your answer should contain circuit diagrams, where appropriate.

Question 3. Convert the Sum of Products expression represented by the minterm list

$$Q = \Sigma m(0, 1, 3, 4, 6, 7, 8, 9, 11, 13)$$

to a Product of Sums expression represented by a Maxterm list.
Draw the circuit which implements the Maxterm list.

Question 4. Convert the following Boolean expression into the Reed-Muller form and then draw the circuit which implements the expression using only AND gates and Exclusive OR gates.

$$Q = A.\overline{B} + B.\overline{C}$$

Question 5. Minimise the function represented by the following minterm list.

$$Q = \Sigma m(26, 43, 49, 53, 81, 82, 85, 90, 107, 111) + d(18, 21, 47)$$

You may use the template below.
Verify your result by carrying out the minimization indicated by the table.
You should return this page, with the table suitably marked, as part of your answer.

Write your name here .....

0	16	48	32	96	112	80	64
1	17	49	33	97	113	81	65
3	19	51	35	99	115	83	67
2	18	50	34	98	114	82	66
6	22	54	38	102	118	86	70
7	23	55	39	103	119	87	71
5	21	53	37	101	117	85	69
4	20	52	36	100	116	84	68
12	28	60	44	108	124	92	76
13	29	61	45	109	125	93	77
15	31	63	47	111	127	95	79
14	30	62	46	110	126	94	78
10	26	58	42	106	122	90	74
11	27	59	43	107	123	91	75
9	25	57	41	105	121	89	73
8	24	56	40	104	120	88	72

Table for Question 5