DUBLIN CITY UNIVERSITY

Summer 2003

COURSE:	APPLIED PHYSICS PHYSICS with a LANGUAGE
YEAR:	2
SEMESTER	2
EXAMINATION:	PS206: Electronics 2
EXAMINER:	Dr B. Lawless Ph 7005300
DURATION:	2 hours
INSTRUCTIONS:	Answer 5 parts of Question 1 (50 %) and 2 other questions (25 % each)

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until instructed to do so.

Total number of pages 5

Question 1. Answer five parts of this question.

(a) What is meant by the acronym CMOS?
What are the main features of CMOS tecnology?
Explain the advantages of using CMOS integrated circuits.

(b) Carry out the following conversions and explain the method in each case.

i. Convert 43981_D to Hexadecimal.

ii. Convert $4CB2F_H$ to Decimal.

iii. Convert 99_D to Gray code.

iv. Convert 85_D to Binary.

v. Calculate the negative of $0B1C2_H$.

(c) Explain how the use of parity check bits can be used to ensure the accuracy of transmitted or stored digital data.

(d) Draw a circuit which implements the truth table shown below. Can the circuit be simplified? How would you test your circuit? Give the minterm list corresponding to this truth table.

A	B	C	Q
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

Truth Table for Question 1 (d).

(e) Draw up the circuit diagram which implements the following Boolean expression

$$Q = A.B + \overline{A}.\overline{B}.C + B.C.\overline{D}$$

(f) State the postulates of Boolean Algebra.
Prove De Morgan's Theorem, $\overline{A + B} = \overline{A}.\overline{B}$.
Give the logic gate symbols which are equivalent to each side of the equation $\overline{A.B} = \overline{A} + \overline{B}$.

(g) Explain the operation of the ttl NAND gate circuit shown in Figure 1.

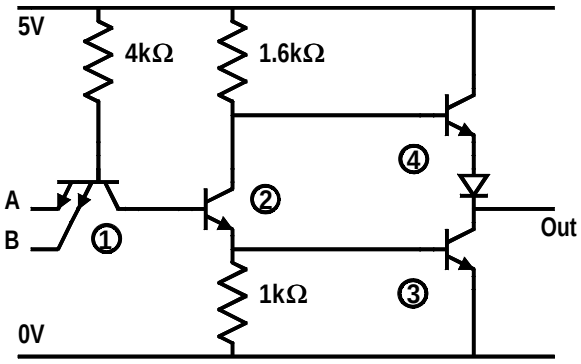

Figure 1: Question 1(g)

(h) Construct the truth table which represents the circuit shown in Figure 2.

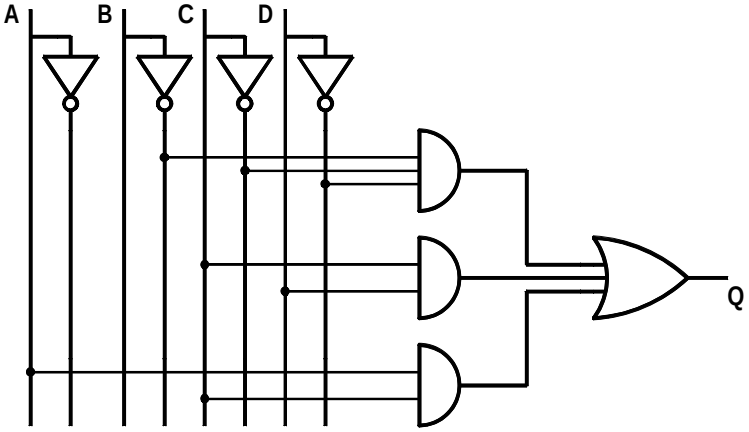

Figure 2: Question 1(h)

Question 2. A particular logic application problem has been specified in the form of a minterm list given by:

$$Q = \Sigma m(0, 4, 6, 9, 14, 22, 23, 27, 30)$$

Using this information you are to:

(a) Draw up the truth table for the system.

(b) Construct the Boolean expression for the system.

(c) Construct the Maxterm list for the system.

(d) Simplify the Boolean expression using any suitable method.

(e) Draw a circuit diagram for the logic gate circuit.

Question 3. Draw the logic gate circuit diagram for an RS flip flop. Give an account in words of the operation of the flip flop.
Construct the Function Table which specifies the operations of the flip flop.
Explain how any ambiguities in the operation of the flip-flop can be removed.
Explain how the RS flip-flop can be converted into a gated D type flip-flop.

Question 4. Discuss the operation of two of the following types of Analog to Digital converters, using flow charts and block diagrams where appropriate.

(a) Ramp type feedback converter.

(b) Successive approximation feedback converter.

(c) Flash converter.

(d) Integrating type converter.

Question 5. What is meant by "The Canonical Form" of an expression?
Use the identity $\overline{X} = 1 \oplus X$ to convert the expression

$$Q = f(A, B, C, D) = A.B.\overline{C}.\overline{D} + \overline{A}.B.C.\overline{D} + A.\overline{B}.C.D$$

into Reed-Muller Canonical form. Draw the circuit which implements the Reed-Muller expression.

Question 6. Identify and correct the errors in the circuits shown below:

(a) The led is to light for $Q = 1$ where $Q = A.B$

(b) The led is to light for $Q = 1$ where $Q = A + B + C$.

(c) The led is to light when $A = B$

(d) The led is to light for $Q = 1$ where $Q = A.B.C$

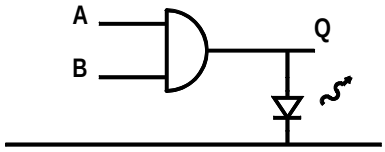

Figure 3: Question 6(a) led ON for $Q = A.B$

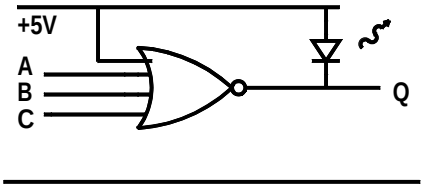

Figure 4: Question 6(b) led ON for $Q = A + B + C$

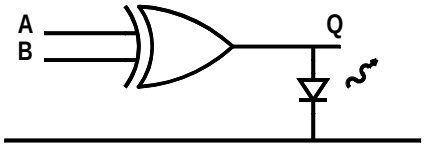

Figure 5: Question 6(c) led ON for $A = B$

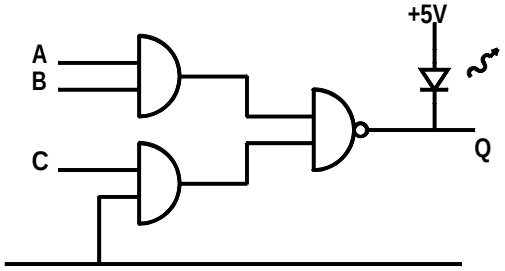

Figure 6: Question 6(d) led ON for $Q = A.B.C$