# DUBLIN CITY UNIVERSITY

**August 2003**

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| COURSE: | APPLIED PHYSICS<br>PHYSICS with a LANGUAGE |
| YEAR: | 2 |
| SEMESTER | 2 |
| EXAMINATION: | PS206: Electronics 2 |
| EXAMINER: | Dr B. Lawless Ph 5300 |
| DURATION: | 2 hours |
| INSTRUCTIONS: | Answer 5 parts of Question 1 (50 %)<br>and 2 other questions (25 % each)<br>Do not turn over this page<br>until instructed to do so.<br>Total number of pages 5 |

**Question 1.** Answer five parts of this question.

(a) Explain the operation of the ttl NOR gate shown in Figure 1. What is meant by "current sinking logic"?

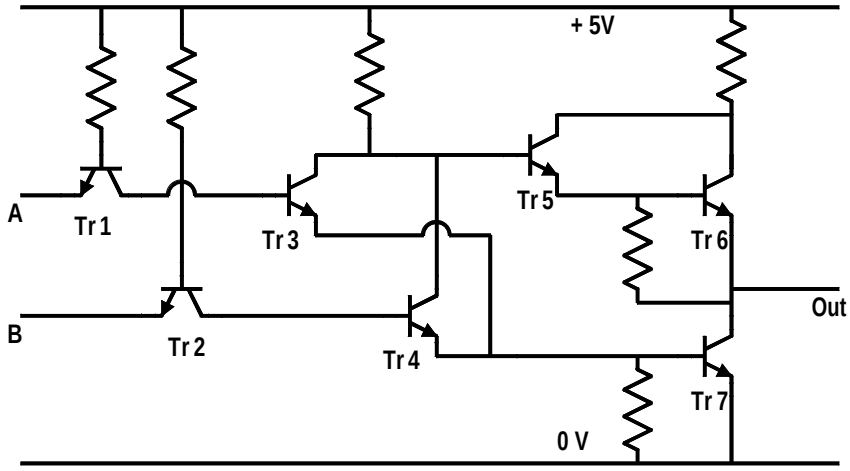


Figure 1: Question 1(a)

(b) What ate the principal differences between ttl and CMOS logic gate circuits?

(c) Carry out the following conversions and explain the method in each case.

i. Convert $703710_D$ to Hexadecimal.

ii. Convert $425D4_H$ to Decimal.

iii. Convert $37_D$ to Gray code.

iv. Convert $95_D$ to Binary.

v. Calculate the negative of $FDCB0_H$.

(d) Draw a circuit which implements the truth table shown below. Can the circuit be simplified? How would you test your circuit? Give the minterm list corresponding to this truth table.

| A | B | C | Q |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |

**Truth Table for Question 1 (d).**

(e) Draw the circuit diagram which implements the following Boolean expression

$$Q = \overline{A.B} + \overline{B + C} + B$$

and give the truth table for this Boolean expression.

(f) What is meant by the terms "Cyclic" and "Reflective" as applied to Gray code? Why is the Gray code system frequently used in angle and position sensors?

(g) Explain what is meant by the term "Canonical Sum of Products" form. Put the following expression into the Canonical SoP form.

$$Q = A.\overline{B} + B.C$$

(h) Construct the truth table which represents the circuit shown in Figure 2.

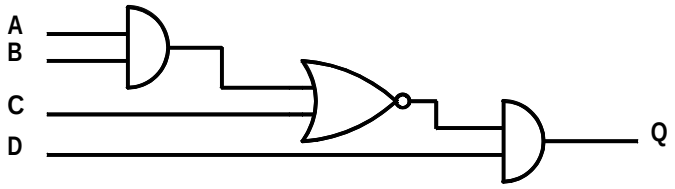


Figure 2: Question 1(h)

**Question 2.** Derive the Maxterm list for the Boolean expression defined by the truth table shown below.
Give the Maxterm list corrsponding to this truth table.
Draw the Karnaugh Map for this truth table and obtain a simplified expression for Q.

| A | B | C | D | Q |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

**Truth Table for Question 2.**

**Question 3.** The logic gate circuit diagram for a JK flip flop is shown in Figure 3. Give an account inwords of the operation of the flip flop.
Explain the operation of the edge triggering part of the flip flop.
What features of the flip flop enable it to be used as a counter?

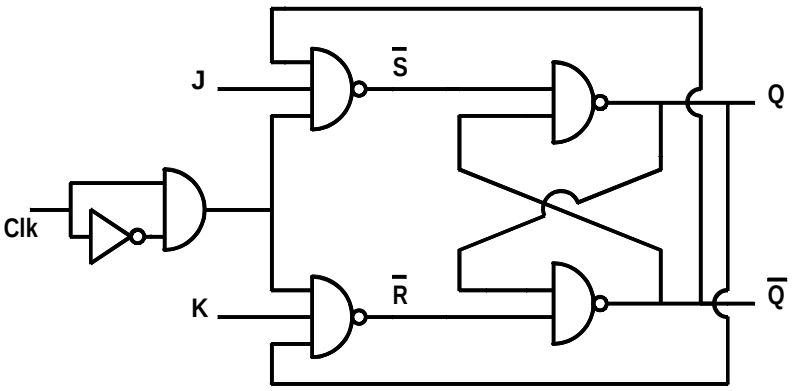


Figure 3: Question 3.

**Question 4.** Use the methods of Boolean algebra to simplify the following Boolean expression:

$$\begin{aligned} Q &= \overline{A}.\overline{B}.\overline{C}.D.\overline{E} + \overline{A}.\overline{B}.C.D.\overline{E} + \overline{A}.B.\overline{C}.D.\overline{E} + \overline{A}.B.C.\overline{D}.E \\ &\quad + A.\overline{B}.\overline{C}.D.\overline{E} + A.B.\overline{C}.D.\overline{E} + A.B.C.\overline{D}.\overline{E} \end{aligned}$$

**Question 5.** Explain the operation of a 555 Timer oscillator. Give a block diagram of the internal circuit blocks of the 555 Timer. Describe, with the aid of diagrams, the waveforms which you would observe with an oscilloscope which is connected to the timing capacitor and the output pin when the circuit is set up as a free running oscillator.

**Question 6.** Explain the operation of the R-2R ladder network used in the D/A converter shown in Figure 4.

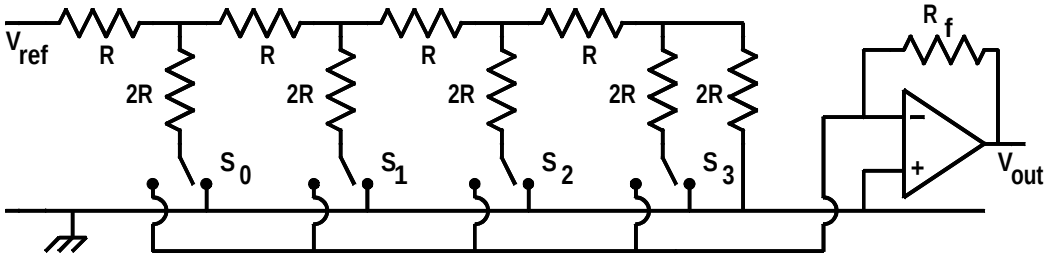


Figure 4: Question 5

Show how this D/A converter can be used to implement an A/D Feedback converter. Discuss the algorithms which are used to control the operation of these feedback A/D converters.