DUBLIN CITY UNIVERSITY

Summer 2002

COURSE:	APPLIED PHYSICS PHYSICS with a LANGUAGE
YEAR:	2
SEMESTER	2
EXAMINATION:	PS206: Electronics 2
EXAMINER:	Dr B. Lawless
DURATION:	2 hours
INSTRUCTIONS:	Answer 5 parts of Question 1 (50 %) and 2 other questions (25 % each)

Do not turn over this page
until instructed to do so.

Question 1. Answer five parts of this question.

(a) Give an account of the principal differences in performance and use of ttl (74 series) and CMOS (4000 series) logic gate integrated circuits.

(b) Explain the meaning of the following terms

i. Propagation delay

ii. Current sinking

iii. Function table

iv. Ohmic contact

v. Schottky diode

(c) Draw a circuit which implements this truth table. Can the circuit be simplified? How would you test your circuit? Give the minterm list corresponding to this truth table.

A	B	C	Q
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

Truth Table for Question 1 (c).

(d) Draw up the truth table which represents the following Boolean expression

$$Q = \overline{A}.B + A.\overline{B}.C + B.C.\overline{D}$$

(e) Carry out the following conversions and explain the method in each case.

i. Convert 39612_D to Hexadecimal.

ii. Convert $1E240_H$ to Decimal.

iii. Convert 132_D to Gray code.

iv. Convert 170_D to Binary.

v. Get the negative of $E5A5_H$

(f) What is the next number in the following sequence and why?
3, 5, 6, 10, 12, ...

(g) Derive the Boolean logic expression which describes the circuit in Figure 1.

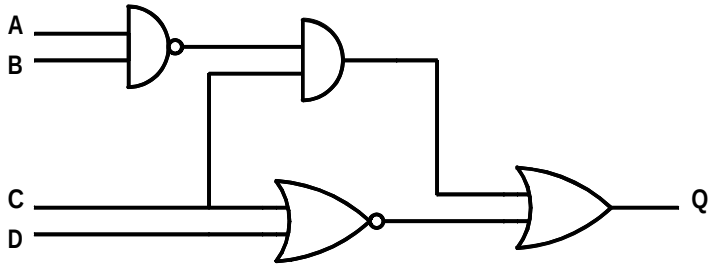

Figure 1: Question 1(g)

(h) Explain, briefly, the concept of Hamming Distance between code words. Show how the introduction of extra parity bits allows both the identification of corrupted data and also correction of the corrupted data if only one data bit has been corrupted.

Question 2. Derive the Maxterm list for the Boolean expression defined by the truth table shown below.
Express Q as a Product of Sums Boolean expression.
Draw the Karnaugh Map.

A	B	C	D	Q
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	1

Truth Table for Question 2.

Question 3. The logic gate circuit diagram for a JK flip flop is shown in Figure 2.
Give an account in words of the operation of the flip flop.
Construct the Function Table which specifies the operations of the flip flop.
Explain the operation of the edge triggering part of the flip flop.
What features of the flip flop enable it to be used as a counter?
Explain the operation of a modulo 10 BCD counter.

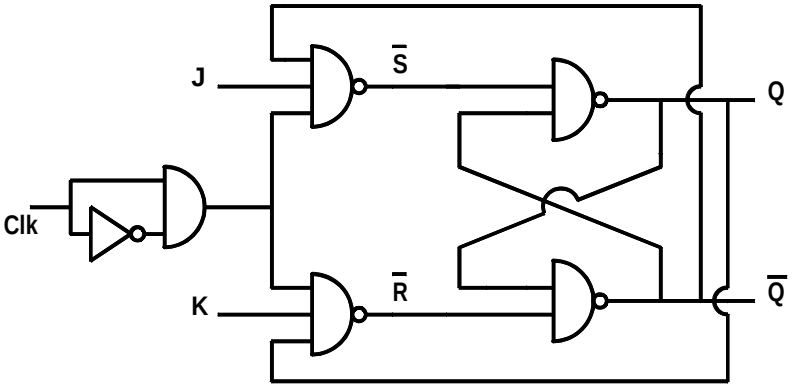

Figure 2: Question 3

Question 4. A function is specified by the minterm list

$$Q = \Sigma m(7, 15, 27, 35, 43, 71, 79, 91, 99, 103, 107, 111)$$

The output BLIF file resulting from an ESPRESSO minimisation is shown below. Provide comments on each line which explain the meaning of the line. Then use the file to draw the minimised logic circuit diagram.

```
.model ap2ex
.inputs v0 v1 v2 v3 v4 v5 v6
.outputs v7.0
.names v0 v2 v4 v5 v6 [1]
10111 1
.names v1 v2 v3 v4 v5 v6 [2]
011011 1
.names v1 v2 v4 v5 v6 [3]
10011 1
.names v1 v2 v4 v5 v6 [4]
00111 1
.names [1] [2] [3] [4] [5]
0000 1
.names [5] v7.0
0 1
.end
```

Question 5. Obtain the minterm list for the expression shown below. Simplify the Boolean expression. You may use the table as an aid.

$$\begin{aligned} Q \quad = \quad & \overline{A}.\overline{B}.C.\overline{D}.\overline{E}.F.G + \overline{A}.\overline{B}.C.\overline{D}.E.\overline{F}.G + \overline{A}.\overline{B}.C.D.E.F.G \\ & + \overline{A}.B.\overline{C}.\overline{D}.\overline{E}.F.G + \overline{A}.B.C.\overline{D}.E.\overline{F}.G + \overline{A}.B.C.D.E.F.G \\ & + A.B.\overline{C}.D.\overline{E}.\overline{F}.G + A.B.\overline{C}.D.E.\overline{F}.G + A.B.C.\overline{D}.\overline{E}.\overline{F}.G \\ & + A.B.C.\overline{D}.E.\overline{F}.G \end{aligned}$$

0	16	48	32	96	112	80	64
1	17	49	33	97	113	81	65
3	19	51	35	99	115	83	67
2	18	50	34	98	114	82	66
6	22	54	38	102	118	86	70
7	23	55	39	103	119	87	71
5	21	53	37	101	117	85	69
4	20	52	36	100	116	84	68
12	28	60	44	108	124	92	76
13	29	61	45	109	125	93	77
15	31	63	47	111	127	95	79
14	30	62	46	110	126	94	78
10	26	58	42	106	122	90	74
11	27	59	43	107	123	91	75
9	25	57	41	105	121	89	73
8	24	56	40	104	120	88	72

Table for Question 5