DUBLIN CITY UNIVERSITY

May 2001

COURSE:	APPLIED PHYSICS PHYSICS with a LANGUAGE APPLIED LANGUAGES EXTERNAL
YEAR:	2
SEMESTER	2
EXAMINATION:	PS206: Electronics 2
EXAMINER:	Dr B. Lawless
DURATION:	2 hours
INSTRUCTIONS:	Answer 5 parts of Question 1 (50 %) and 2 other questions (25 % each)

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until instructed to do so.

Question 1. Answer five parts of this question.

(a) Sketch and explain the operation of a ttl NAND gate integrated circuit. Explain the function of the two emitters on the input transistor. What is meant by "current sinking logic"?

(b) Sketch and explain the operation of a CMOS NAND gate integrated circuit. Discuss the advantages and disadvantages of using CMOS integrated circuits.

(c) Carry out the following conversions and explain the method in each case.

i. Convert 12692_D to Hexadecimal.

ii. Convert $0110\ 1101\ 1011\ 0000_B$ to Decimal.

iii. Convert 19_D to Gray code.

iv. Convert $7AE34_H$ to decimal.

(d) Explain what is meant by the terms "Cyclic" and "Reflective" as applied to Gray code. Why is the Gray code system sometimes used in sensors?

(e) Draw the logic gate circuit implementation of:

$$Q = A.\overline{B} + \overline{A}.B + A.B.\overline{C} + \overline{A}.C$$

(f) Derive the Boolean logic expression which describes the circuit in Figure 1.

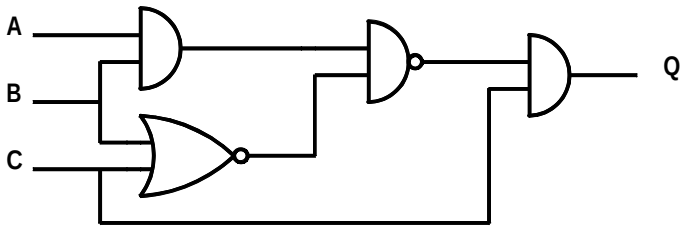

Figure 1: Question 1(f)

(g) Draw a circuit which implements the system described by the truth table shown below:

A	B	C	Q
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Truth Table for Question 1 (g).

(h) Simplify the following expression using Boolean algebra:

$$\begin{aligned} Q &= \overline{A}.\overline{B}.\overline{C}.D + \overline{A}.\overline{B}.C.D + \overline{A}.B.\overline{C}.\overline{D} + \overline{A}.B.\overline{C}.D \\ &\quad + \overline{A}.B.C.\overline{D} + \overline{A}.B.C.D + A.\overline{B}.\overline{C}.D + A.B.\overline{C}.D \end{aligned}$$

Question 2. Draw the Karnaugh Map for the truth table shown below. Use the map to obtain a simplified expression for Q.
Explain how the Karnaugh Map method works and outline the limitations of the method.
Give the minterm list corresponding to this Truth Table.

A	B	C	D	Q
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	1

Truth Table for Question 2.

Question 3. Explain how a Sum-of-Products Boolean expression can be put into the Reed-Muller form by use of the identity:

$$\overline{X} = 1 \oplus X$$

Convert the following expression into the Reed-Muller form.

$$Q = A.\overline{B} + A.B.\overline{C} + \overline{A}.C$$

Draw the circuit which implements this Reed-Muller expression.

Question 4. Explain the operation of an RS Flip Flop with particular reference to the effects of the introduction of feedback.
Show how the indeterminate state is avoided by the inclusion of the inverter in the D type Flip Flop shown in Figure 2.
What modifications should be made to the circuit in Figure 2 in order to change the circuit into a gated or clocked D type Flip Flop?

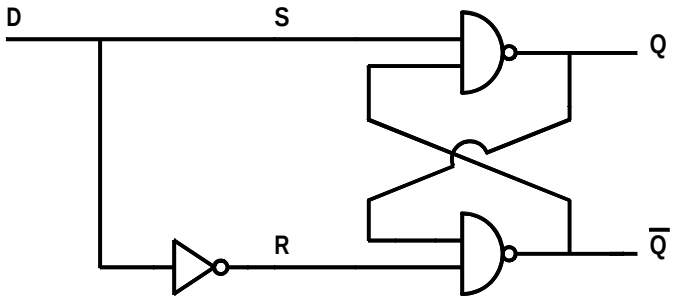

Figure 2: Question 4.

Question 5. Explain the operation of the 4 bit, R-2R ladder network used in the D/A converter shown in Figure 3.

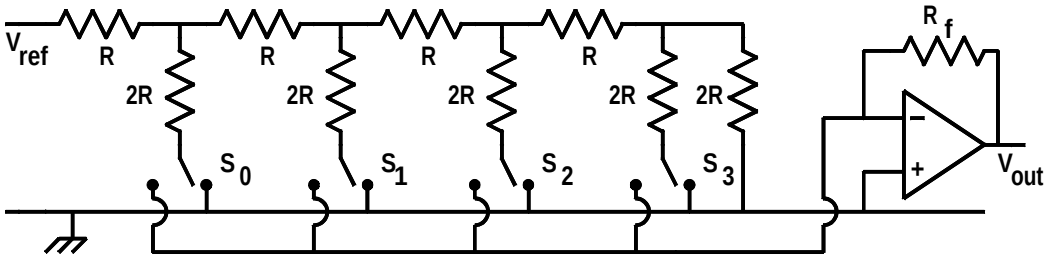

Figure 3: Question 5

Give an account of the operation of the algorithm which is used in the feedback successive approximation A/D converter which uses this R-2R Ladder.
A particular 8 bit A/D converter has a range of 0.0 to 1.0 V. What change in the input voltage which will cause a least significant bit change in the output? What is the largest change in the input voltage which will cause only one least significant bit change in the output? What will be the binary output when an input voltage signal of 0.38 V is digitised?