DUBLIN CITY UNIVERSITY

Summer 1997

COURSE: APPLIED PHYSICS

PHYSICS with a LANGUAGE

YEAR: 2

EXAMINATION: Physics B: Electronics

EXAMINERS: Prof. C. Lewis.

Prof. D. Williams Dr B. Lawless

DURATION: 3 hours

INSTRUCTIONS: AP students: Answer FIVE questions

PL students: Answer FOUR questions

- Question 1. A potential divider is formed from two impedances, Z_1 and Z_2 , as shown in Figure 1. Channel A of an oscilloscope displays the waveform at point A and Channel B displays the waveform at point B. Give scaled sketches of the oscilloscope waveforms, showing the amplitude and phase of the signals when:
 - (a) Z_1 is a resistance of value $1k\Omega$, Z_2 is a resistance of value $4.7k\Omega$ and f=1kHz.
 - (b) Z_1 is a capacitor of value $0.3\mu F$, Z_2 is a resistance of value $2.2k\Omega$ and f=200 Hz.
 - (c) Z_1 is a resistor of value 820 Ω , Z_2 is an inductor of value 20mH and $f=5{\rm kHz}$.

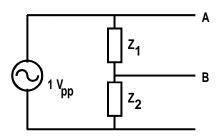


Figure 1: Question 1

Question 2. Explain what is meant by a Thévenin equivalent circuit. What conditions must apply before a Thévenin equivalent circuit can be obtained?

When an oscilloscope was connected across the output of a particular circuit, a 3.9 V_{pp} sinusoidal waveform at a frequency of 1.5kHz was obtained. When a load resistor of 50 Ω was connected across the output, the waveform observed was a 2.7 V_{pp} sinusoidal waveform at a frequency of 1.5 kHz. Calculate the Thévenin equivalent of the circuit.

Question 3. The circuit in Figure 2 shows a junction FET amplifier. Describe and explain a design procedure for determining the values of R_G , R_S , R_D and the supply voltage. Obtain values of R_G , R_S , R_D , C_{in} , C_{out} and C_S so that the amplifier will have an input impedance of $500\text{k}\Omega$, a midband gain of -7 and a low frequency 3dB cutoff at $400\,\text{Hz}$.

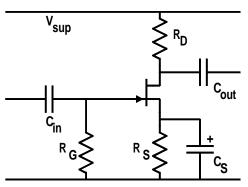


Figure 2: Question 3

Question 4. Explain the following phenomena in terms of the solid state physics of semiconductor materials and device structures:

- (a) Variation of junction capacitance as a function of diode voltage.
- (b) The positive temperature coefficient of resistance of metals and the negative temperature coefficient of resistance of semiconductor materials.
- (c) The increase of reverse leakage current of a diode with increasing temperature.
- (d) The reverse breakdown mechanisms in a Zener diode.
- (e) The operation of an npn transistor.

Question 5. Analyse the two adder circuits shown in Figure 3 and obtain expressions for the output voltage in terms of the input voltages and the circuit resistors. Give a test matrix of input voltages and the expected output voltages which will check the functioning of the circuit and the linearity of the circuit. Explain what circuit characteristic is checked in each row of the test matrix.

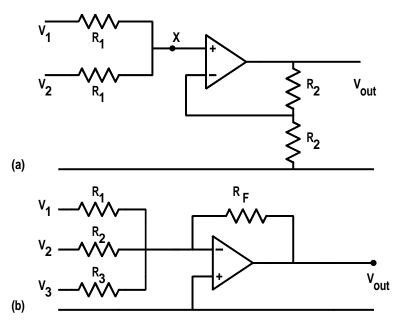


Figure 3: Question 5

- Question 6. (a) Explain the operation of an R—2R digital to analog converter. Give a sketch of a suitable circuit as part of your answer.
 - (b) Explain the operation of an integrating analog to digital converter. Give a sketch of a suitable circuit as part of your answer.

The minterm specification for a logic gate system is given by: Question 7.

$$Q = \Sigma m(0, 2, 7, 9, 12, 14, 15)$$

Give the truth table for the system.

Obtain a Karnaugh map for the system and thence obtain a minimized expression for Q.

Write the Boolean algebra expression for Q and use the methods of Boolean algebra to simplify the expression.

Show that the Karnaugh map method and the Boolean simplification methods can give the same simplified expression.

Question 8.

- (a) Explain the following terms as they apply to a 8255 interface chip on a compuer interface card.
 - i. Base address
 - ii. Port address
 - iii. Mode control word
 - iv. Input/Output
 - v. Bit set mode

Write a C program to configure and control Port A (at address 644) so as to operate a set of traffic lights at crossroads in the normal red/green/orange sequence.

(b) Write a PSPICE input file to model the circuit shown in Figure 4. The program should plot the transient response of the circuit for a sinusoudal input signal of amplitude 10 V and for frequencies between 10 Hz and 20 kHz.

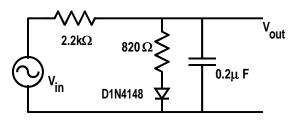


Figure 4: Question 8