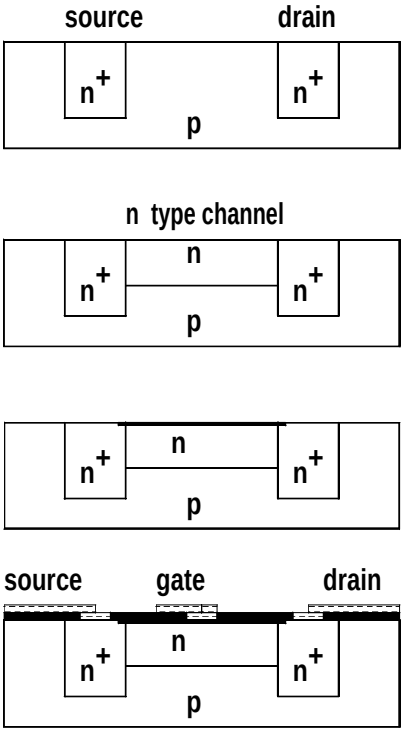
The depletion type MOSFET conducts for a gate to source voltage of zero.
It is a **normally on** device.
Drain current drops to zero at $V_{GS(off)}$.

The enhancement type MOSFET does not conduct for a gate to source voltage of zero.
It is a **normally off** device.
The device starts to conduct at $V_{GS(th)}$.

CMOS devices use complementary p and n channel enhancement type MOSFETs in the one integrated circuit of two or more MOSFETs.



Two heavily doped (+) n type wells called source and drain are formed in lightly doped p type substrate

A lightly doped n type channel is formed, which joins the two wells.

A thin layer of oxide is formed over the channel region

A metal gate electrode is applied over this thin oxide layer on the channel.

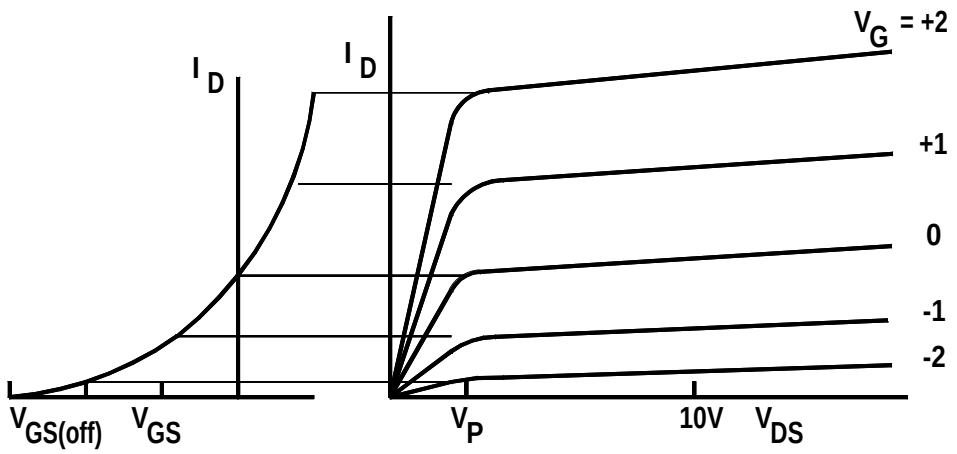
A covering oxide layer is applied and windows etched in oxide. Metallic contact tracks are laid down to make contact to the source, gate electrode and drain

n channel depletion mode MOSFET

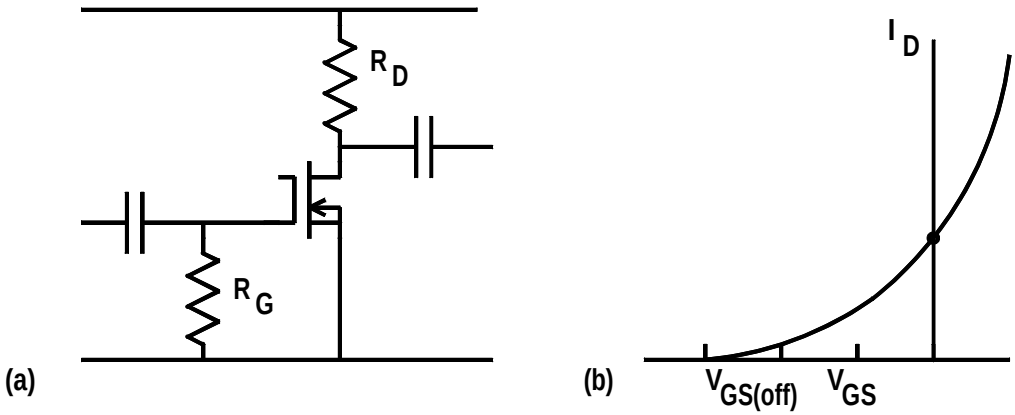
MOSFET = Metal Oxide Silicon Field Effect Transistor

IGFET = Insulated Gate ...

Source and drain are heavily doped, isolated regions or wells on the wafer.
n channel depletion mode MOSFET has fabricated channel
n channel enhancement mode MOSFET has no fabricated channel
Thin layer of silicon dioxide formed over the channel
Metallised gate region is formed on the silicon dioxide over the channel
Thick silicon dioxide protective overlayer
Windows etched through silicon dioxide for metal contacts to n^+ source and drain wells and to the gate
No conducting path between the gate lead and the channel.
Possible static damage to thin gate layer of SiO_2.



n channel depletion mode MOSFET
Negative voltage applied to the gate, MOSFET operates in depletion mode
Positive gate voltage, the MOSFET operates in enhancement mode
1. Electrons attracted into the channel by the positive gate voltage
2. Holes in the substrate are repelled from under the gate giving an increase of electrons in the channel
Semiconductor equation, $n \times p = n_i^2$
If p decreases in $n \times p = n_i^2$ then n increases.



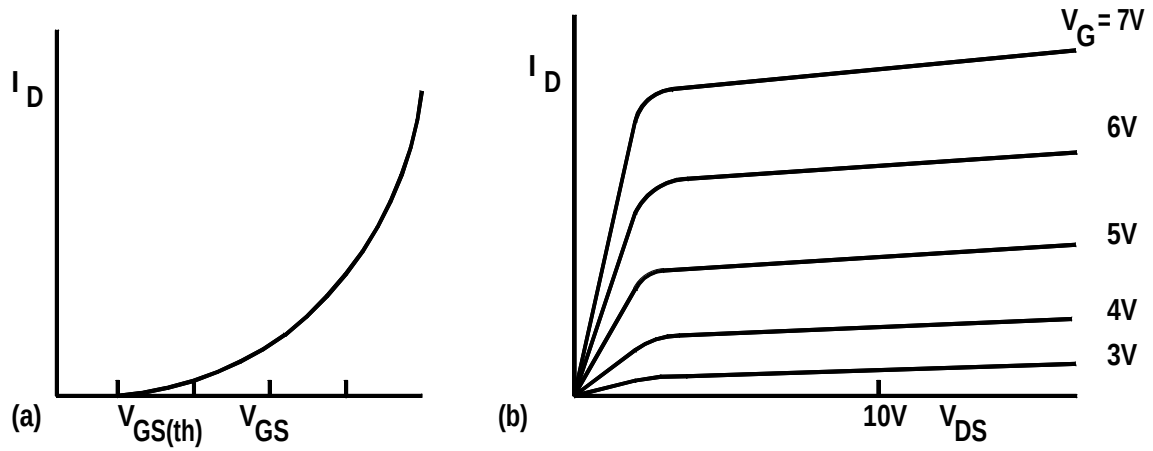
Basic MOSFET amplifier circuit and input characteristic

Advantage of either polarity gate voltage is that no gate bias is required

Simplifies use of MOSFETs in integrated circuits.

Depletion mode MOSFET symbol has continuous bar for channel

n channel arrow points to channel



The enhancement mode MOSFET

The n channel enhancement mode MOSFET is fabricated without a doped n type channel connecting the n^+ source and drain wells. Requires a threshold voltage V_{th}. Semiconductor equation, $n \times p = n_i^2$, then gives an increased electron concentration which results in the formation of an n type channel connecting the source to the drain.

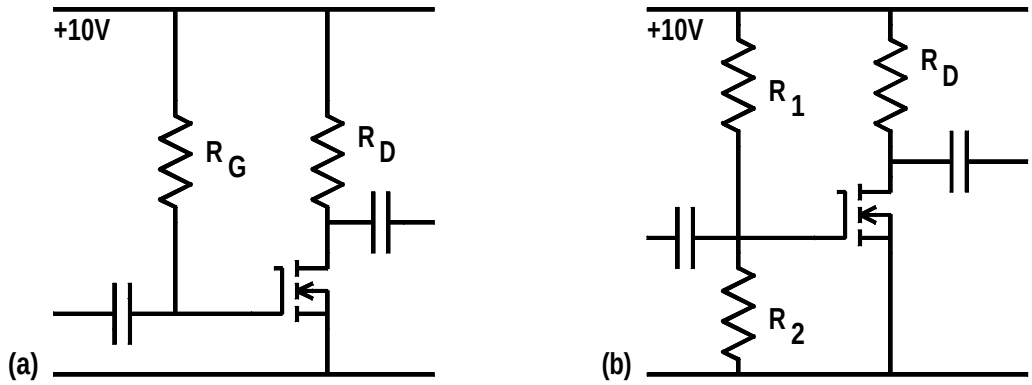
Enhancement type MOSFETs require a gate voltage in excess of the threshold voltage

Once conduction occurs between the source and drain, the current in the drain in the saturation region is given by the equation

$$I_D = k(V_{GS} - V_{th})^2$$

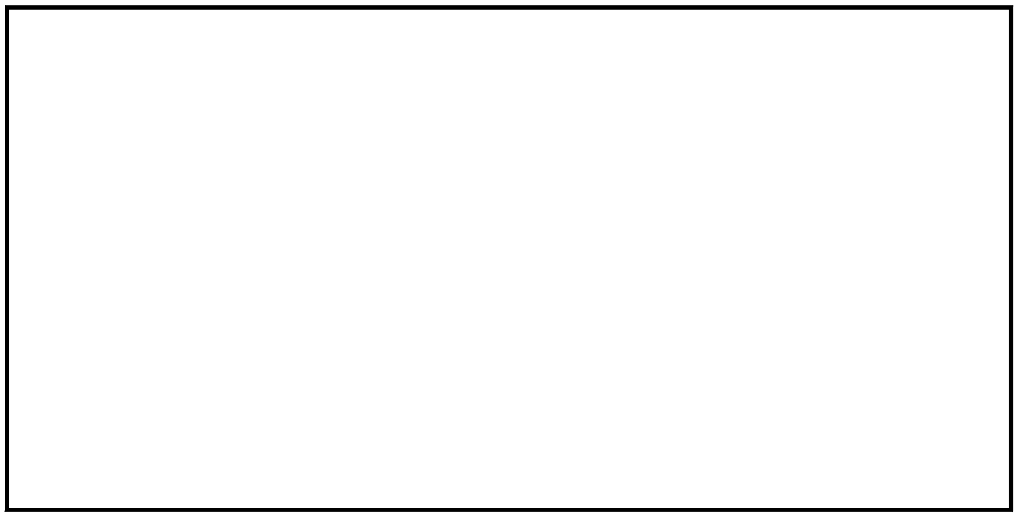
where k is a constant for the particular MOSFET in use.

It is not possible to use the concept of I_{DSS} for an enhancement type MOSFET since there is no current for zero gate to source bias.



Two types of enhancement MOSFET bias circuit
Symbol for the enhancement type MOSFET has interrupted bar for the channel.

The supply voltage must be greater than the threshold voltage.
The main advantage of MOSFET devices for analogue electronics is the very high input resistance

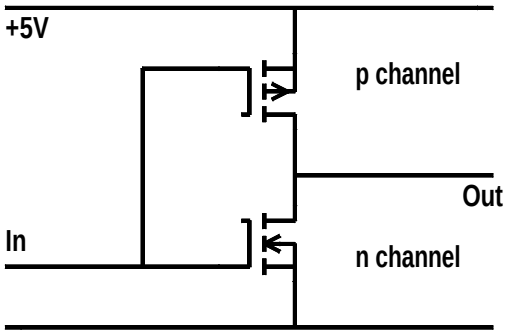


CMOS = Complementary Metal Oxide Silicon FETS

p and n channel MOSFETs fabricated side by side on the same wafer

In general the MOSFETs are used as active load type devices where load resistors are replaced by MOSFETs.

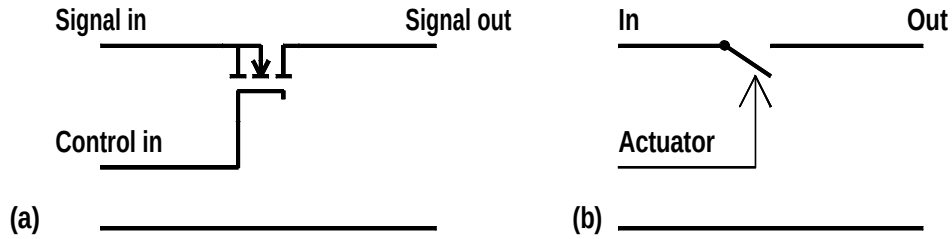
Low quiescent currents



CMOS inverter

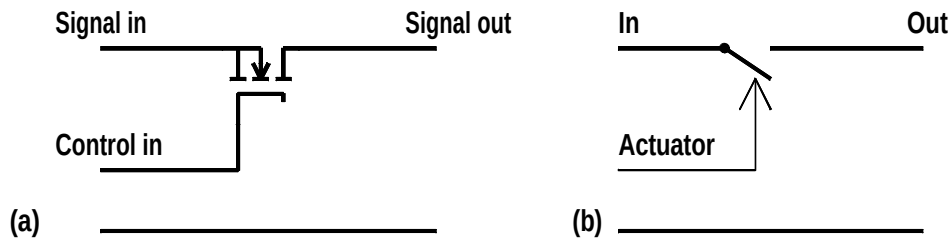
p channel MOSFET at the top and an n channel MOSFET is used at the bottom. Two drains are connected together

$0V$ in gives V_{sup} out, V_{sup} in gives $0V$ out. One of the MOSFETs is always off so no quiescent current which makes circuit suitable for use in battery powered devices.



MOSFET analogue switch using an enhancement type MOSFET.

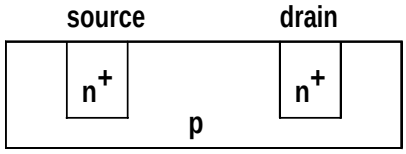
The input signal in the range -5V to +3V. Calculate the output voltage for a load resistor of $10k\Omega$ when the control input is at -5V and when the control input is at +5V. The threshold voltage for the MOSFET is +2V.



Control is isolated from the signal which is being switched.

Control input is at -5V, no channel is formed between the source and the drain and the switch is OFF.

Control input is at +5V, the resistance between the source and drain is low, the switch is ON. Available as an integrated circuit (CMOS 4066B type device)



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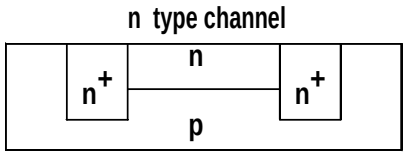

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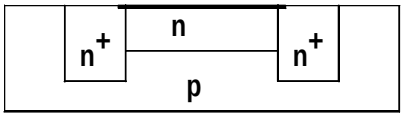

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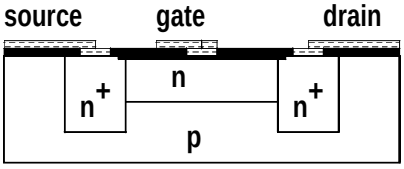

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