In the semiconductor fabrication process

- Silicon dioxide is an insulator
- Silicon dioxide can be formed on silicon substrates
- Etchant preferentially dissolves silicon dioxide
- Photoresist protects the oxide from being etched.
- Oxide protects dopant from reaching the silicon.

In JFET operation

- Increasing drain to source voltage gives increased drain current.

- Increasing drain voltage pinches off the conduction channel and reduces the drain current.

- These two processes partially cancel out.

A JFET is specified by three parameters:—

$V_{GS(off)}$ = Gate-Source cut off Voltage

I_{DSS} = Drain Saturation current for zero Source to gate voltage

$g_m = \frac{dI_D}{dV_{GS}} =$ mutual conductance

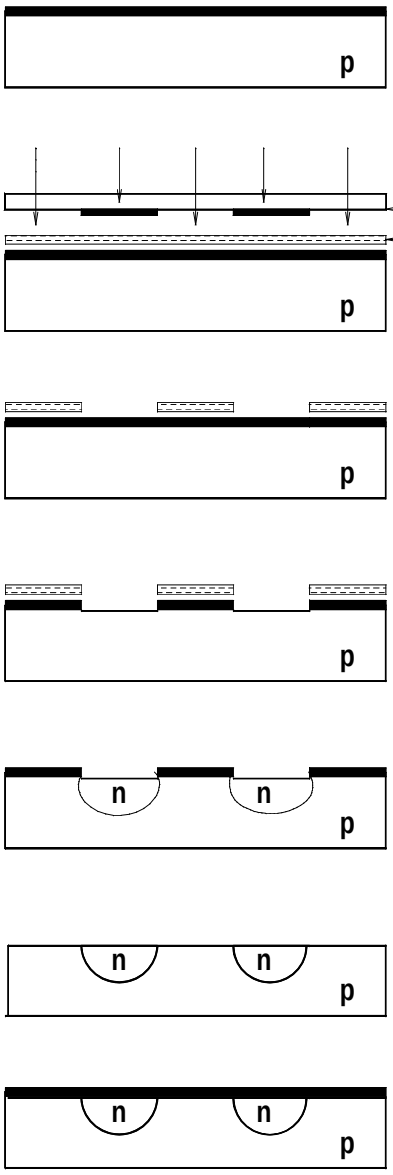
Unit Operations in fabrication.

Silicon wafer is a 0.5mm thick, 100mm, 150mm or 200mm diameter disk of silicon sliced, parallel to a crystal plane, from a large, raw crystal or boule of high purity, lightly doped p or n type silicon.

Thin native oxide layer of SiO_2 about 0.1nm thick. Thickness of dioxide can be increased by Heating to 1000K in steam and oxygen.
Electrochemical anodisation
Plasma reaction.
Deposition of oxide by Chemical Vapour Deposition in which silane (SiH_4) gas is reacted with oxygen gas.

Silicon dioxide, (essentially a layer of glass) can be dissolved by etching in hydrogen fluoride (HF)
HF does not dissolve silicon.

A photoresist is an organic material
Spun-on to the wafer surface to give a layer about a micron thick.
Negative photoresist exposed to ultraviolet light polymerises and hardens
In the developing process, unexposed, unpolymerised photoresist is dissolved and removed
Exposure through a photomask which is a patterned layer of metal on a glass substrate.
To leave a hardened resist pattern coating the wafer with a pattern which is the negative of the metal pattern on the mask.



p type wafer substrate with 1μm oxide layer

Ultraviolet light exposure

Mask pattern on glass support

Spun on photoresist layer

Mask pattern in developed photoresist

Windows etched in oxide not protected by photoresist

n type dopant diffused into silicon through windows in oxide

Etch the oxide and reoxidise

Repeat the process with a different mask pattern.

Photolithography using a negative photoresist

Oxide layer in the regions not protected by hardened photoresist is etched away either by immersing the wafer in HF or by use of a plasma etcher.
Windows formed in the oxide in the same pattern as the original metal pattern on the mask.
On completion remaining photoresist os removed by a plasma ashing process or by a wet chemical process.

The wafer is then placed in a furnace in an atmosphere of either p type (boron) or n type (phosphorous) dopant containing gas.
The dopant enters the silicon wafer through the windows in the oxide and diffuses down into the wafer.
The wafer is protected from the dopant gas in the other regions by the oxide.

Remove photoresist and etch oxide
Grow new oxide layer and repeat with different mask pattern
Form structured layers on silicon wafer.
Also form Metal layers and layers of polysilicon
Connections e made to specific doped regions
Connecting tracks can cross if polysilicon is used as an insulating layer

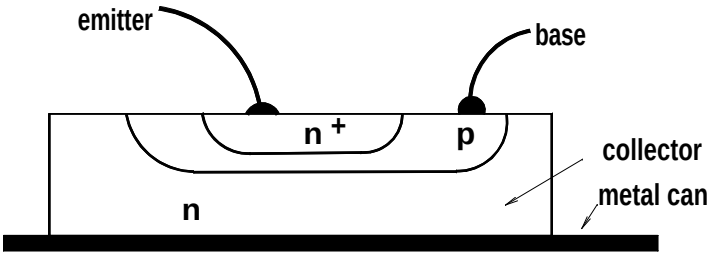
Capacitors formed by placing an oxide layer between two metallic layers.
Form resistors from controlled tracks of p or n type silicon
Multiple copies possible
Scribe and dice the wafer
Clean rooms No dust to cause unwanted masking.

Bipolar transistors

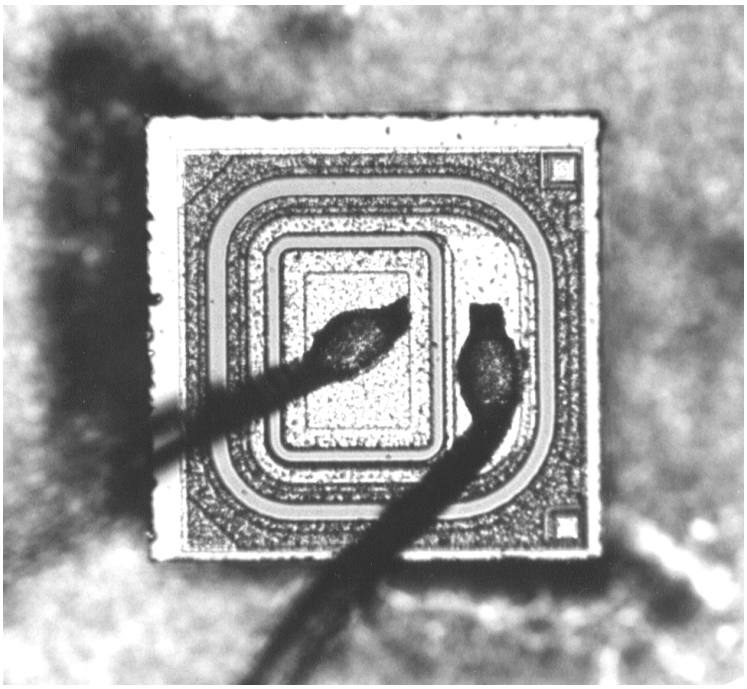
In principle can be formed with two masks

In practice more needed to obtain protective oxide over-layer with windows for metallic coating to which contacts are made

The emitter region starts out as n type substrate,
It is then doped p type during the base region formation
And is turned back to n type by further doping during the emitter region formation.



Cross section of an npn transistor



Microphotograph of a BC109 transistor

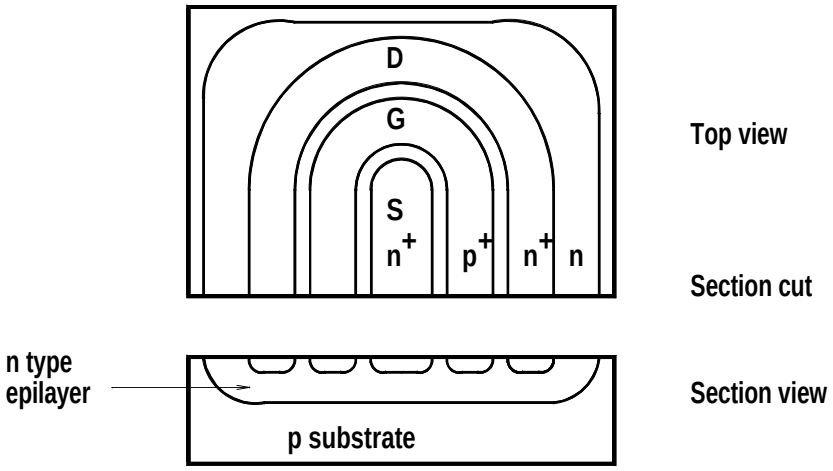
Connections made using thin gold wire welded to metal pads on the base and emitter and to the lead out wires

The collector, substrate, bonded to metal can which forms third connection and a heat sink.

If current is too large connecting wires of small signal transistors heat and fuse giving an open circuit

Simple tests for diode action can usually verify the functioning of signal transistors.

Leads of power transistors are usually heavier and do not fuse so the semiconductor can overheat and change in performance and degrade

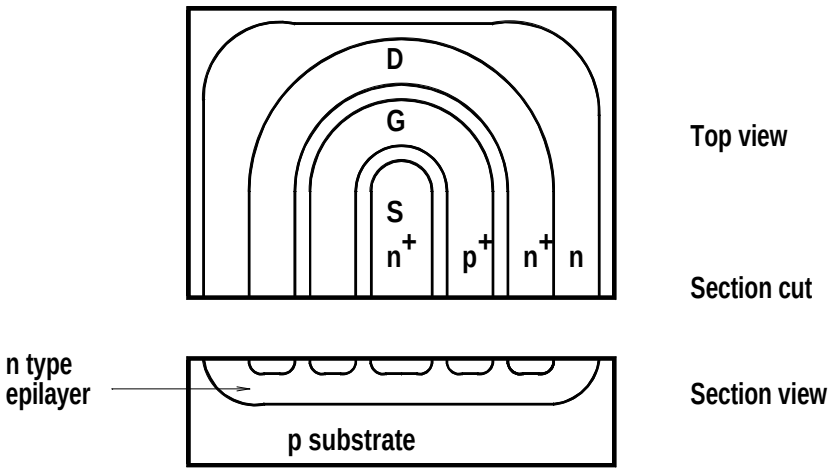


Structure of an n channel JFET

The unit processes involved in the manufacture of JFETs and bipolar transistors are the same.
But a different arrangement of masks is used to give a different geometry for JFETs.

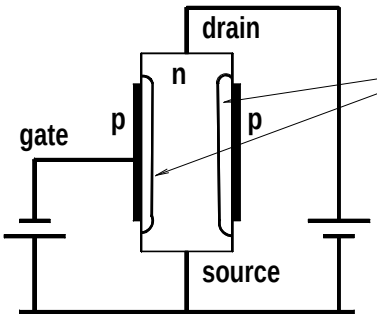
The conduction path from the source to the drain is along the n channel between the gate and the p type substrate
Since it is necessary to prevent the source and drain from coming into contact, the device is fabricated as an annulus as shown.
There is then no end to the gate and drain regions at which the source could short to the drain or to the substrate.

The essential difference between the bipolar transistor and the FET is that the current flows perpendicularly through the thin base region in the bipolar transistor and but along the channel in the case of the FET.

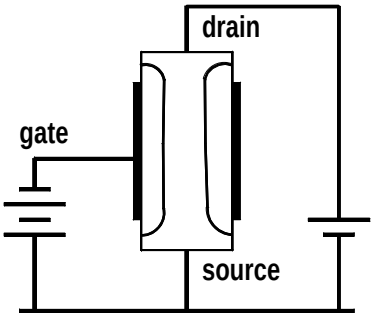


Consider a radial section through the device

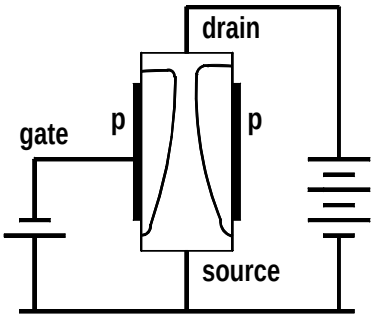
The depletion layer associated with the heavily doped p type gate region extends into the channel.
Reverse bias applied to the gate region constricts the channel
The FET is a voltage controlled device whereas the bipolar transistor is a current controlled device.



Depletion layer formed due to reverse biased channel to gate and channel to p type substrate junctions

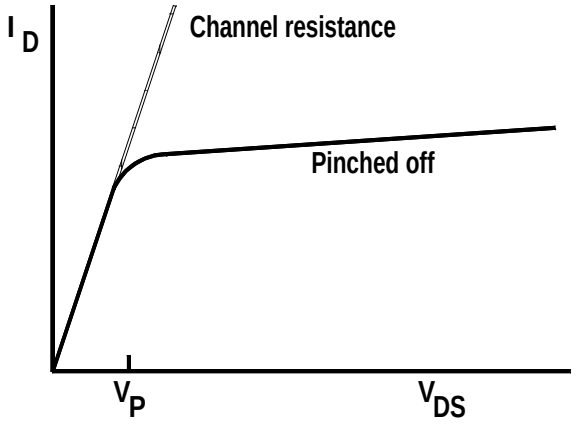


As the gate reverse bias is increased the depletion layer becomes thicker reducing the width of the conducting channel and therefore reducing the current flowing for a particular source to drain voltage

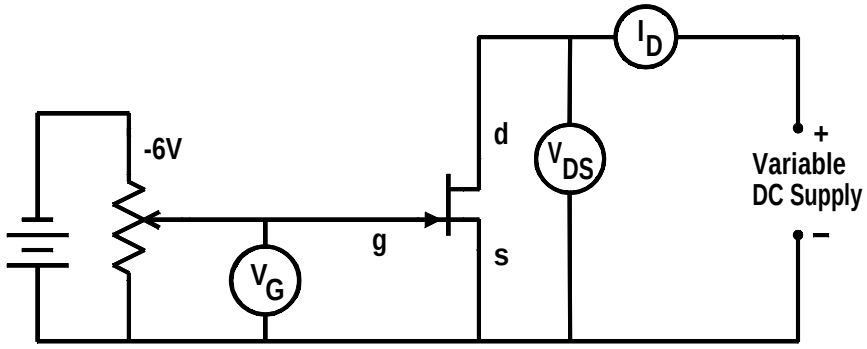


As the source to drain voltage is increased the depletion layer at the drain end of the channel becomes thicker due to the greater reverse bias at that end of the channel. This reduction of channel width tends to balance the greater current due to the greater voltage along the channel.

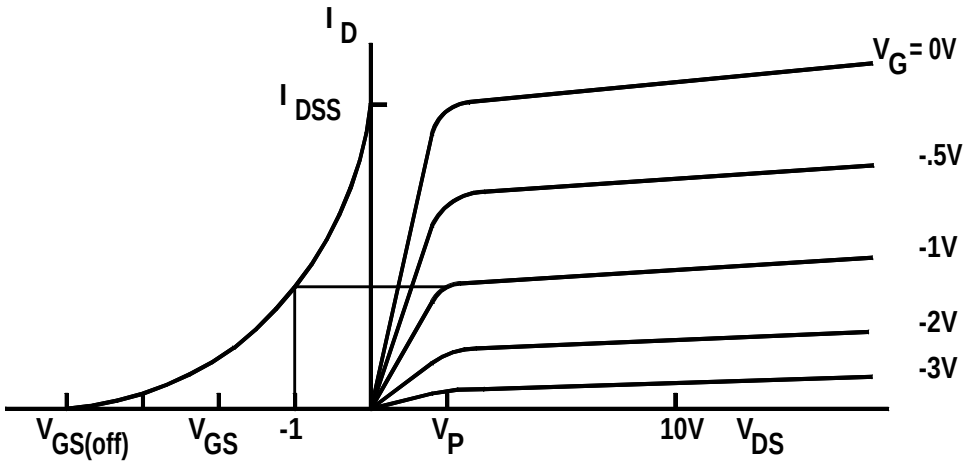
Mechanism of operation of a JFET



Effect of the pinch off mechanism
Another mechanism operates.
For voltages greater than what is called the Pinch Off Voltage, V_P, applied between the source and the drain, the increased reverse bias between the upper end of the gate and the drain gives a thicker depletion layer at the top of the channel.
which counteracts the increased current which would otherwise flow from the source to the drain.

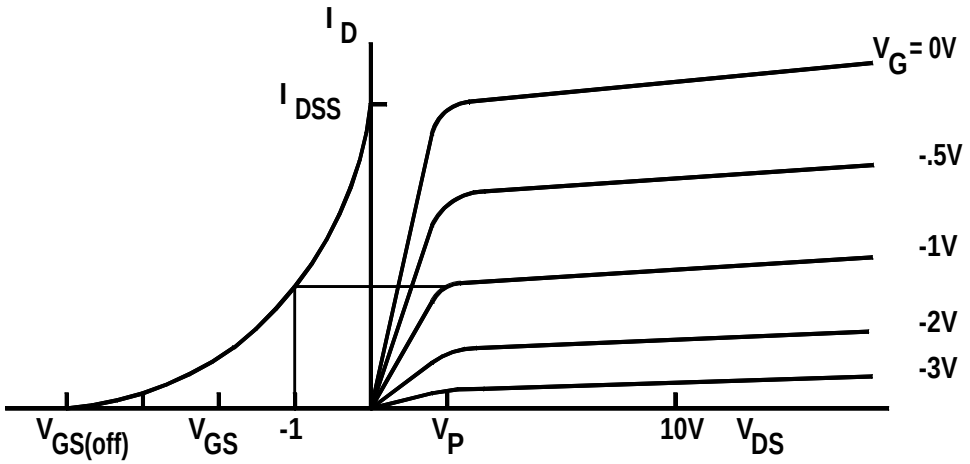


Circuit for measuring JFET characteristics of 2n3819



The general shape is a rising region followed by a saturated region in which the current is pinched off.
For a gate to source voltage of 0V, the drain current is a maximum called I_{DSS}, the Drain Saturation current.

The gate to source voltage at which the drain current drops to 0mA is called the Gate-Source cut off voltage, $V_{GS(off)}$.



Theoretical analysis yields

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

The slope of this curve is the mutual conductance, g_m, for the JFET.
The quoted value for g_m for the 2N3819 JFET is $g_m = 2000\mu S$ (micro Siemens) at $V_{DS} = 5V$.
The Siemen is the unit of conductance and has units of $\frac{\text{Amps}}{\text{Volts}}$.