Unit 27 Asynchronous sequential circuits

- If there is feedback in a circuit, then the circuit will have a memory and can not be expressed as a Boolean Sum of Products.
- Asynchronous sequential circuits do not wait for a clock pulse before changing the output.
- Asynchronous sequential circuits change the output one propagation delay time after the primary input changes.
- The system will only be in a stable state if the next state and the present state are the same.
- Stable states are those states for which the q values in the **Excitation map** are the same in each column.
- The **flow table** shows the sequence of stable states.
- The flow table allows the preparation of the **State diagram**.

This is an appropriate point at which to obtain an overall view of the course. The structure divides roughly into three sections:

1. Combinational logic circuits in which the outputs are determined only by the inputs at that instant and there is only one output set associated with a particular set of inputs. It is assumed that sufficient time is allowed for any switching transients to have died away. Various minimization techniques are available which allow for circuit minimization or simplification. Essentially these circuits can be described in terms of a look-up table where a particular output is obtained by looking up the input combination. An example would be a combination lock in which three numbers must be set up on three different dials before a safe will open.
2. In sequential circuits an output waveform pattern or sequence results from a train or sequence of input pulses. Typical circuits are the various form of flip flop and counter circuits discussed in Units 22 to 26. These

circuits are clocked circuits in that the input data is read on a clock edge. The example here would be a combination lock which has one dial and the first number is set up and read at time zero, the second number is read at time 10 seconds and the final number is set up and read at time 20 seconds.

3. Asynchronous sequential circuits are also circuits which respond to a sequence of input pulses but there is one important difference; the circuits are asynchronous or non clocked so the inputs are read as soon as they are changed. Since it is not possible to change two inputs simultaneously the circuit can only follow a trajectory which is associated with only one input variable changing at a time. Two adjacent inputs can only differ in one variable. As a result of this, particular output states may be reached by a number of different trajectories and also it may only be possible to reach particular states by following a definite trajectory. The example here is a single dial on the lock. You turn to the first number, stop then turn to the second number, stop and then turn to the third number in order to open the safe. You can pause for as long as you like at each stage. It is only important that the correct sequence is entered.

In an asynchronous sequential circuit feedback is used in the same way as it was used to generate the latching action in the RS flip flops which we discussed in Unit 22. However, there is no clock signal to gate the reading of the feedback signal. There is always some delay, either actually present or present by implication, in the feedback signal path from the output back to the input as shown in Figure 27.1.

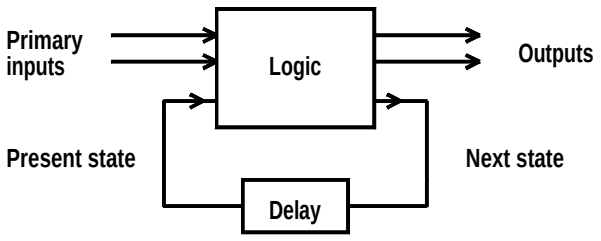

Figure 27.1:

In this circuit, the next state output will, after the propagation delay time, arrive at the present state input and be fed through the logic circuit

to generate the new output. The system will be in a stable state if the next state and the present state are the same.

A practical example of such a circuit is shown in Figure 27.2. Here we have broken the feedback loop at the point marked Link so that we can determine the forward signal by imposing an input at q and comparing it to the feedback signal:

$$Q = \overline{\overline{A.B}.\overline{B.q}} = A.B + B.q$$

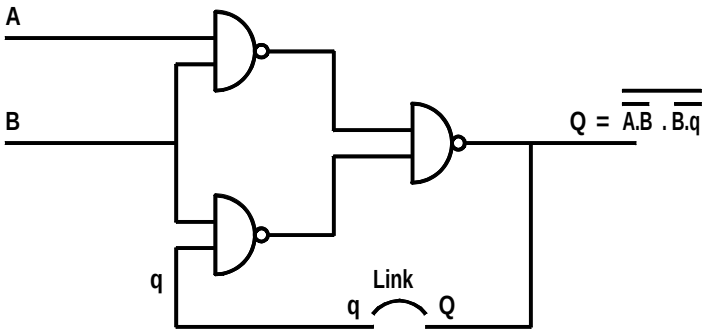

Figure 27.2:

We now prepare what is called an **Excitation Map** of this circuit. The various primary inputs are assigned at the tops of the columns. The two possibilities for the present state inputs with the circuit in open loop are assigned to the rows as shown in the table below. The entries in the various positions in the body of the table are the output values of Q from the circuit as determined by $Q = AB + Bq$.

	AB			
	00	01	11	10
$q = 0$	0	0	1	0
$q = 1$	0	1	1	0

Excitation Map for Q

The stable states are those states for which $Q = q$ that is those states which have 0's in the top row and 1's in the bottom row of the excitation table. For these stable states, closing the loop will have no effect since the signals are the same at each side of the loop. However for the state in the top row for which the inputs are $A = 1$, $B = 1$ and $q = 0$, the output is $Q = 1$ so the state is unstable and either q or Q must change. A and B are fixed externally so that any change must occur in the vertical direction in

the table, after the loop is closed at the link. After one time delay the new value of q will be that of Q, that is $Q = q = 1$ so that the system has jumped from the top row to the bottom row and it can be seen that this will give a stable state.

The **Flow table** is now prepared by circling the entries in the excitation for which $Q = q$ which are all stable states of the system. These stable states are then given identification numbers and a flow table is prepared as shown below:

	AB			
	00	01	11	10
$q = 0$	(1)	(2)	4	(5)
$q = 1$	1	(3)	(4)	5

Flow Table.

In this flow table the state number 4 appears twice, In the upper row it is an unstable state for which $Q \neq q$ which only occurs for one cycle before the system jumps to the stable circled state 4 in the lower row for which $Q = q$. For state 5 the jump is in the up direction to give a stable state in the upper row. The two states 2 and 3 are both stable and are therefore both circled as shown.

In this flow table there are five stable states which we will now represent as five circles on the partial state diagram shown in Figure 27.3. A state diagram is an example of a directed graph with each node representing a circuit state and each edge representing a transition from one state to another.

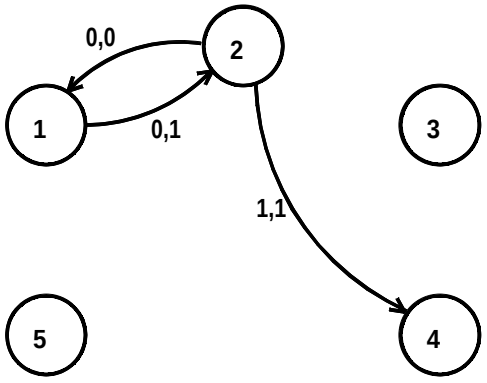

Figure 27.3: Partial state diagram.

In this partial state diagram we have only shown the interaction associated with the state which has been labeled 2 in the flow table. In state 2 $A = 0$, $B = 1$ and $Q = 0$. The primary inputs, A and B can be each changed by external action but changing either input will cause the system to jump to a different state so we need to consider changing only one of A or B. If the primary inputs are changed from 0,1 to 0,0 the system jumps from state 2 to state 1 without change of Q. This is represented by the arc with 0,0 written beside it joining state 2 to state 1. If the primary inputs are changed from 0,1 to 1,1 the system jumps from state 2 to the metastable state 4 and thence to the stable state 4 represented by the circled 4 in the flow table and by the circle in this partial state diagram. This is represented by the arc with the 1,1 written beside it which joins state 2 to state 4. Note that in this state transition there is a change in the output value from $Q = 0$ to $Q = 1$. The only route by which state 2 can be reached is from state 1 which has primary inputs 0,0. When the 0,0 is changed to 0,1 the system jumps to state 2 as shown by the arc from 1 to 2 with 0,1 written beside it.

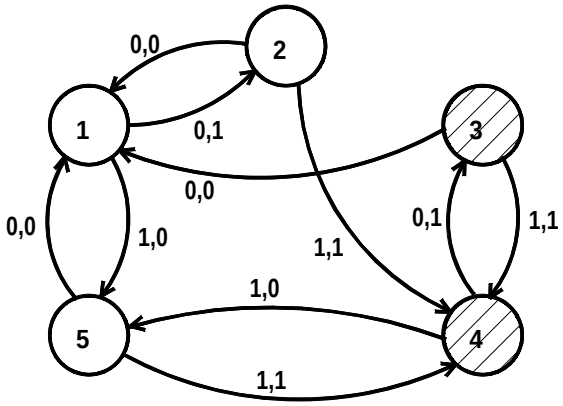

Figure 27.4: Complete state diagram.

If there are two adjacent stable states in the same row of the flow table, then there a reversible path between those two states represented by two arrowed arcs in the state diagram. If a transition between two adjacent columns of the flow table is accompanied by a change of the output Q then there is an intervening metastable state associated with the change of row and then this is indicated on the state diagram by a single arrowed arc and also the path is non reversible.

For simplicity, in Figure 27.3 we only showed the transitions to and from state 2. When all of the other possible transitions are included we get the full state diagram shown in Figure 27.4. We have also indicated the value of

the output Q for a particular state on this diagram by the hatching of the circle when the state has an output of $Q = 1$.

It should also be noted that when there are more than the two inputs, A and B, it will not be possible to use Gray code sequencing for the AB columns in the Flow Table. This is the same problem as was discussed in Unit 15.

27.1 References

Beards, Peter H (1997) *Analog and digital electronics*, Prentice Hall

Lala, Parag (1996) *Practical digital logic design and testing* Prentice Hall.

27.2 Examples

27.1 Obtain the Boolean expression for the open loop version of this feedback circuit.
Prepare the excitation map, flow table and state diagram.

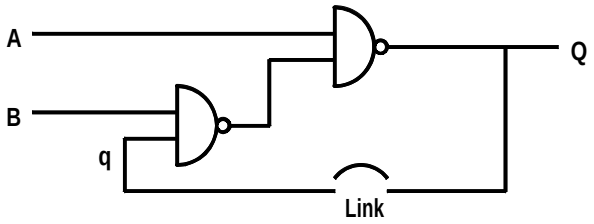

Figure 27.5: RS flip flop diagram.

The expression for the circuit output, Q, is:

$$Q = \overline{\overline{B.q}.A} = \overline{A} + \overline{\overline{B.q}} = \overline{A} + B.q$$

This allows us to prepare the excitation map:

	AB			
	00	01	11	10
$q = 0$	1	1	0	0
$q = 1$	1	1	1	0

Excitation Map for Q

and the flow table:

	AB			
	00	01	11	10
$q = 0$	1	2	⑤	④
$q = 1$	①	②	③	4

Flow Table.

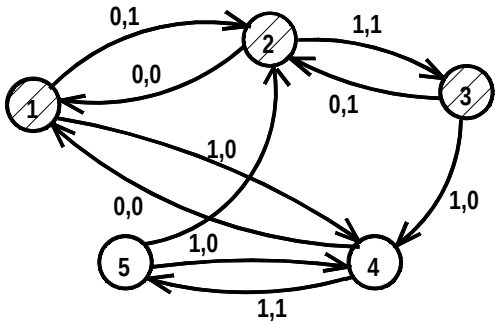

Figure 27.6: State diagram.

27.3 Problems

27.1 Show that the output of the circuit in Figure 26.2 is:

$$Q = \overline{\overline{A.B}.\overline{B.q}} = A.B + B.q$$

27.2 In the system represented by the state diagram shown in Figure 26.5, is it possible for the system to go directly from state ② to state 3?

27.3 A cup of coffee from a machine costs 60 c. Coins for 5 c 10 c 20 c and 50 c may be used. No change is given. Draw a state diagram which shows all of the possible intermediate states on the path to the state where at least 60 c has been inserted into the machine and a cup of coffee is then poured for the customer.