

Unit 26 Sequential circuit models.

- Sequential circuits contain memory devices and have a state memory.
 - Synchronous sequential circuits move from one memory state to another under the control of a set of inputs and at a time determined by an external clock.
 - Sequential circuits are modeled by **Mealy** or by **Moore** machine models.
 - The state machines are described either by **state tables** or by **state diagrams**.
 - Procedures exist for converting between Mealy and Moore machine models.
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A sequential circuit is a circuit which follows through a sequence of states with the sequence being determined by the inputs to the circuit and by the present circuit state. This dependence on the present circuit state implies that the circuit has a memory of its state which is stored from the time of the previous clock. These sequential circuits therefore make intensive use of clocked flip flops with the D or J and K inputs to the flip flops being used to determine the transitions which occur. The counters which we examined in the last unit are good examples of sequential machines with the count being used as a clock input.

In this Unit we will examine the formal description or structure of these sequential circuits in terms of state machines.

There are two formal descriptions of these sequential machines called **Mealy machines**, shown in Figure 26.1, and **Moore machines**, shown in Figure 26.2.

In the Mealy machine model the present output state is determined by the present external inputs, the Primary Inputs, and also by the state memory after the previous clock cycle. It can be seen from the block diagram in Figure 26.1 that the inputs can bypass the state memory and cause changes to the output without the occurrence of a clock pulse.

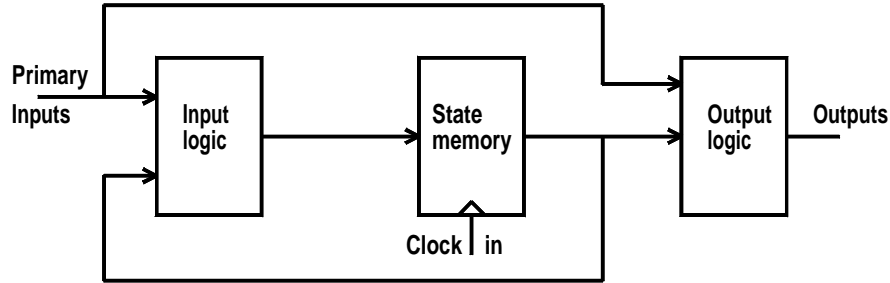


Figure 26.1: Mealy machine model.

In the Moore model the output is determined only by the present state memory which depends on the Primary Inputs at the time of the last clock pulse. There is no bypass path for the external primary inputs directly to the output logic. The Moore machine model is therefore a special case of the Mealy model.

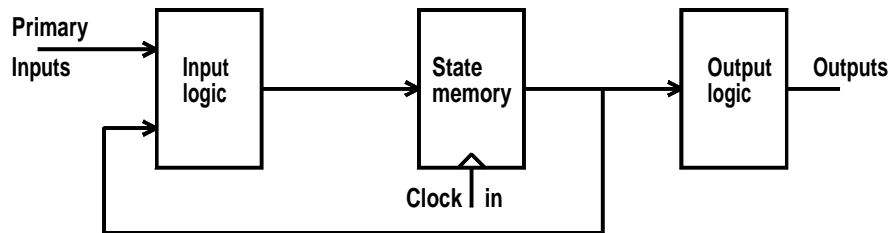


Figure 26.2: Moore machine model is a special case of Mealy machine.

Both machines have a feedback from the state memory output back to the input logic so that in both cases the new state memory output will be determined by the primary inputs in conjunction with the old value of the state memory output.

In the case of the Mealy machine the output can change when the external input changes without any delay for a clock pulse. In the case of the Moore machine, the output can only change as a result of a clock pulse.

A simple example of a sequential machine circuit is shown in Figure 26.3. We have a single input, X , and a single output, Z , from the circuit. The circuit has a single memory cell in the form of a D type positive edge triggered flip flop.

The output from this circuit following a clock edge is determined by the present state of the circuit memory and also by the input, X , to the circuit. Any description of the state of the circuit must contain information of the

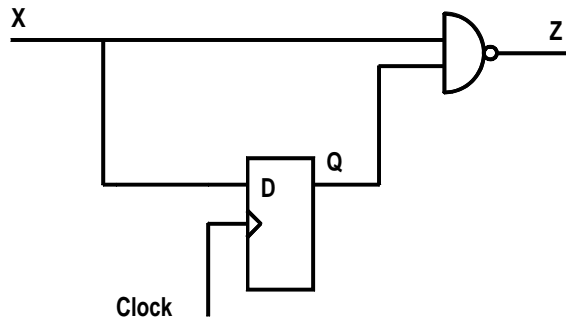


Figure 26.3: Example of simple sequential machine.

next state following a clock edge and also the present output from the circuit, Z . This is presented in the form of (Next State, Output). We therefore prepare a **state table** for the circuit which contains this information in a standard layout. The Mealy model state table for the circuit in Figure 26.3 is shown in the following table.

Present state Q	Input	
	X = 0	X = 1
0	0,1	1,1
1	0,1	1,0

When the input is $X = 0$ the table entries for the next state and output, (Q,Z) , must be $(0,1)$ because a 0 is read into the flip flop and the NAND gate must also give a $Z = 1$ output, irrespective of the previous value of Q .

When the input is $X = 1$, the table entry for the next state, (Q,Z) , is $(1,0)$ when the present state is $Q = 0$ and $(1,1)$ when the present state is $Q = 1$.

In order to facilitate discussion of the state memory of the machine, it is convenient to label the various memory states with letters or names. This is a particular advantage when the state memory consists of a number of binary bits.

The rows of the state table are labeled, usually with letters, as shown in the redrawn state table below. Each row has an identifying labeling letter but all of the states or letters do not have to appear in the entries for the next state in the state table. In this table A corresponds to $Q = 0$ and B corresponds to $Q = 1$.

Present state Q	Input	
	X = 0	X = 1
A	A,1	B,1
B	A,1	B,0

A Moore model leads to a more straightforward state table and state diagram representation since each row (present state) of the state table has only one possible output set whereas the Mealy model rows can have a number of possible outputs depending on the inputs since the inputs can bypass the memory states as was shown in Figure 26.3. Therefore, a Moore model for the example of the D type flip flop system in Figure 26.3 would have a truth table:

Present state Q	Input		Output
	X = 0	X = 1	
A	A	C	1
B	A	B	0
C	A	B	1

where the states are now defined by $Q = (\text{Memory state}, \text{Output})$, that is, $A = 0,1$, $B = 1,0$ and $C = 1,1$.

Another representation of this circuit is in the form of a **state diagram**. A state diagram for the Mealy model of the system is shown in Figure 26.4. The distinct memory states are represented by labeled circles and the transitions are represented by edges connecting the states. The numbers beside the edges are the input and output in form X/Z .

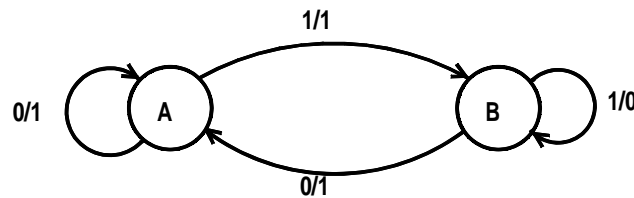


Figure 26.4: Mealy state diagram representation

If the system is in memory state A and an input of 0 is applied, the system goes to state A with an output of 1, represented by the loop on the left with the 0/1 beside it. If the system is in state A and an input of 1 is applied, the system goes to state B with an output of 1 represented by the upper arc with 1/1 beside it.

There are a number of different forms and conventions for drawing state diagrams. In this version, the labels, A and B, represent the state of the internal memory of the system, that is, the state of the D type flip flop. The output from the system is represented by the second term of the number attached to the edges leading to the state. In the example, state A always has an output of 1 because the two edges leading to state A both have /1

beside the edge. The state B can give either output 0 or 1 depending on the last edge which was traversed.

In order to make this Mealy machine concept more concrete we can consider the operation of type 74LS76A type JK flip flop integrated circuit for which the function table quoted by the manufacturer (Texas) is:

Inputs					Outputs	
Preset	Clear	Clock	J	K	Q	\overline{Q}
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\overline{Q_0}$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	$\overline{Q_0}$	Q_0
H	H	H	X	X	Q_0	$\overline{Q_0}$

Function table for 74LS76A JK flip flop

The Mealy machine model for this JK flip flop is shown in Figure 26.5. In this figure the J and K inputs go to the input logic and thence to the state memory. The Preset and Clear go to both the input logic and state memory and also directly to the output logic. The first three rows of the function table show that the Preset and Clear affect the output Q and \overline{Q} as soon as they are applied irrespective of the state of the clock. (X in the function table denotes a “don’t care” condition).

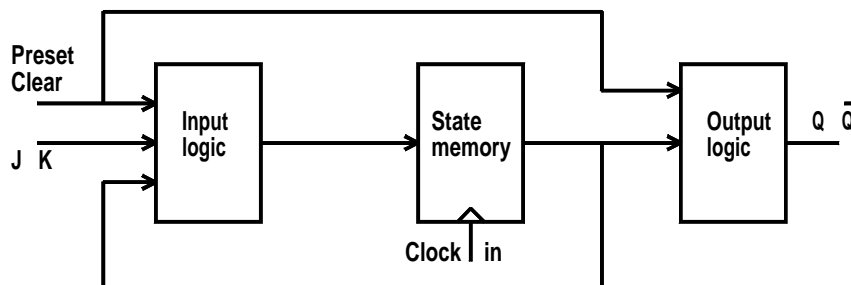


Figure 26.5: Mealy machine model for JK flip flop.

It is a straightforward operation to convert between Moore and Mealy models of synchronous systems as long as you remember two consequences of the bypass of the state memory shown in Figures 26.1 and 26.2.

1. A Moore model has a unique set of outputs for each internal memory state whereas the Mealy model does not.
2. The conversion from the Mealy model to the Moore model does not fully allow for the fact that the output of the Mealy model can change at times other than at the clock edge due to a change in the inputs bypassing the memory state and going directly to the output.

Mealy to Moore model conversion for m memory bits, i inputs and n output lines. Start with the Mealy state table in which each row represents one of 2^m state memories, where each input column represents one of the 2^i possible input combinations and where there are 2^n possible outputs corresponding to the n output lines.

The conversion starts with a Mealy model state table as shown in the example below;

Present state	Input	
	X = 0	X = 1
A	D,0	E,0
B	A,1	A,0
C	B,1	C,1
D	A,0	B,1
E	C,0	D,0

Mealy circuit state table

The entries in the Mealy table are in the form (Next state, Output). The conversion procedure involves identifying all of the distinct sets of (Next state, Output) combinations which occur in the table and generating a row in the Moore state table for each combination. The (Next state, Output) combinations which appear in this Mealy state table are:

A,0	A,1	B,1	C,0	C,1	D,0	E,0
P	Q	R	S	T	U	V

and these form the set of rows for the Moore state table. The Output column of the Moore state table then contains the appropriate output value for that pair. The Mealy state table shown above therefore converts to the Moore state table below and it is evident that the process is an expansion process in that the number of rows increases.

Present state	Input		Output
	X = 0	X = 1	
A,0	D,0	E,0	0
A,1	D,0	E,0	1
B,1	A,1	A,0	1
C,0	B,1	C,1	0
C,1	B,1	C,1	1
D,0	A,0	B,1	0
E,0	C,0	D,0	0

Equivalent Moore circuit state table

which gives, when we use the new labels which combine memory state and output value:

Present state	Input		Output
	X = 0	X = 1	
P	U	V	0
Q	U	V	1
R	Q	P	1
S	R	T	0
T	R	T	1
U	P	R	0
V	S	U	0

Equivalent Moore circuit state table

This last form is convenient for use in drawing the state diagram for the system as shown in Figure 26.6.

Moore to Mealy conversion is carried out by combining the next state columns with the output columns so as to generate a (Next state, output) pair which is entered into the Mealy state table. In the illustration below, the output of 0 for row D are combined and where a D appears in the Moore state table, a D,0 is entered into the Mealy state table.

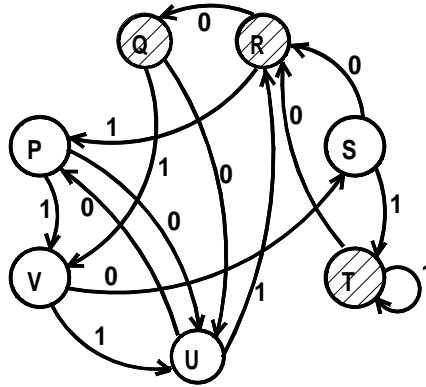


Figure 26.6: Complete state diagram (Moore model).

Present state	Input		Output
	X = 0	X = 1	
A	B	A	0
B	E	F	1
C	D	B	1
D	C	A	0
E	A	D	0
F	E	C	1

Moore circuit state table

In this Moore to Mealy conversion, the number of rows decreases due to the more compressed form of the Mealy state table representation.

Present state	Input	
	X = 0	X = 1
A	B,1	A,0
B	E,0	F,1
C	D,0	B,1
D	C,1	A,0
E	A,0	D,0
F	E,0	C,1

Equivalent Mealy circuit state table

26.1 Examples

26.1 Construct the state diagram for a JK flip flop using a Moore model. Assume that the Preset and Clear are not used.

Since the Preset and Clear are not used, the only transitions that can occur are those which are initiated by the clock edge and therefore the Moore model can be applied.

Since we are using a Moore model, we can use a slightly simplified version of the state diagram representation. The output only depends on the internal state memory and therefore there is a unique output for each memory state so that we can represent the output by overprinting a dot or hatch pattern on the circle representing the state when the output is a 1.

The sequence of construction of the state diagram is shown in Figure 26.7. At the side of each partial state diagram are shown the input values of J and K which give the transitions shown in the state diagram. In particular, the transitions shown in partial diagram (d) represent the toggling action between the two output states.

The transitions associated with the four values of JK are shown in (a) through (d). These transitions are combined in the one state diagram in (e). When transitions along the same edge are combined we get the state diagram shown in (f) in which the pairs of numbers 1,0 etc beside the edges indicate the JK values associated with those transitions.

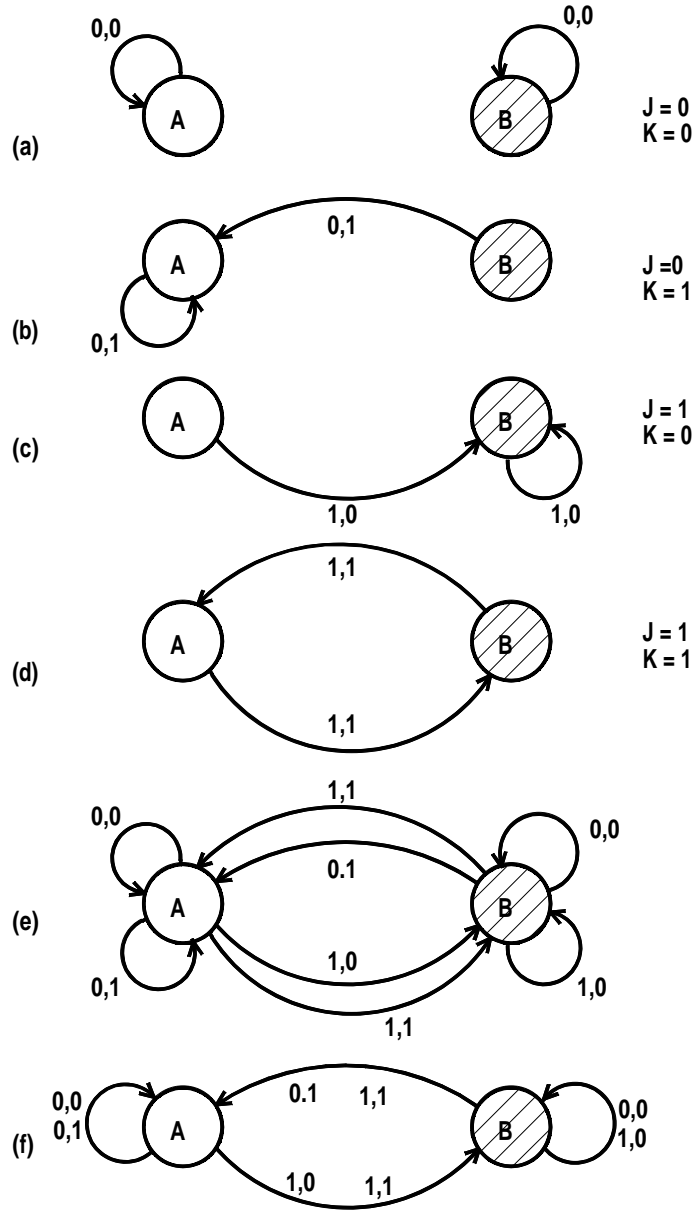


Figure 26.7: Complete state diagram (Moore model).

26.2 Problems

26.1 Construct the state diagram for the Moore circuit state table shown below:

Present state	Input		Output
	X = 0	X = 1	
A	B	A	0
B	E	F	1
C	D	B	1
D	C	A	0
E	A	D	0
F	E	C	1

Moore circuit state table

26.2 Convert the Mealy model shown below to a Moore model and draw the complete state diagram.

Present state	Input	
	X = 0	X = 1
A	C,0	D,0
B	C,1	C,0
C	B,0	E,1
D	B,0	A,1
E	B,0	A,0

Mealy circuit state table