Unit 24 Modulo n Counters

- Base 2 binary counters can be used to construct base m counters by a Clear instruction when the modulus is reached.
- A Down counter counts down from an initial binary number when the $\overline{Q}$ output of the binary counters is used for interstage transfer.
- The count ripples through asynchronous counters.
- All of the stages of a synchronous counter change state at the same time.

In this unit we will investigate some of the other forms of counters, besides binary counters, which are in frequent use. We will also investigate some of the methods used for displaying the output count to the user.

The toggling action of the JK flip flop with $J = K = 1$ allows us to implement binary counters which count up to any number $\leq 2^n - 1$ by using n JK flip flops. The count will however be in binary. It is more convenient for human users if the count can be obtained in some other modulus such as modulo 10 or base 10 and the count then presented in base 10 form.

The use of NAND gates allows the introduction of gated reset which gives a modulo m counter where $m < 2^n$ and n is the number of JK flip flops which are connected in series in the counter. It is therefore a relatively straightforward matter to implement an up counter in which successive clock or count inputs cause the count registered to increase in the natural binary sequence until the modulus is reached which then causes a reset to 0 of the binary counter.

A suitable circuit for a a single stage of a modulo 10 counter is shown in Figure 24.1. Each stage consists of a JK flip-flop with $J = K = 1$ (not shown on diagram). Multiple copies of this circuit are connected in series so as to give multi decade counters.

In this counter, when the output $Z = 1001$ is reached the next count will give the output $Z_{10} = 1010$ which is not permitted in base 10 counting so the NAND gates generate a reset to zero, or a Clear signal, which is applied to the four binary counters. The negative going edge of the A output when

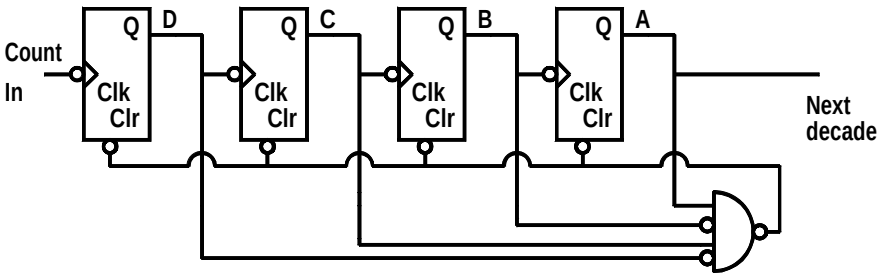

Figure 24.1: Base 10 counter.

the counters are reset to 0 also gives a negative clock or count input into the next decade of a multi decade counter.

Counting in any other base or modulus is achieved by selecting the inputs to the NAND gate so as to generate a reset signal when the modulus is reached.

The circuit for a 3 bit binary up counter is shown in Figure 24.2 (a) together with the timing diagram for the counter.

A down counter is a counter in which the output binary number decreases with successive count inputs. The key to building a down counter is to use the complement, $\overline{Q}$, output to transfer the count to the next binary JK flip flop with the flip flops initially preset to a $Q = 1$ output. The circuit for 3 bit binary down counters is shown in Figure 24.2 (b) together with the timing diagram for the counter. If the initial count is required to be other than 111 then the Preset and Clear of the individual stages can be used to set the initial conditions.

In the down counter, it should be noted that the count outputs are the Q outputs from the JK flip flops, labeled A, B and C but that the count transfer is taken from the complementary outputs. This explains the count advance occurring on the positive going edge of the output even though negative going edge type flip flops are used. All of the JK flip flops are operated in toggling mode but the $J = K = 1$ connections are not shown on the diagram for simplicity.

It is more useful to have a counter which allows for either up or down counting, a reversible counter, and the circuit for such a counter is shown in Figure 24.3. The u/d input allows the direction of count to be switched as required. The AND/OR gates select the signals applied to the clock inputs from either the Q or the $\overline{Q}$ outputs from the flip flops.

Examination of the circuit shows that it is a combination of the two circuits shown in Figure 24.2.

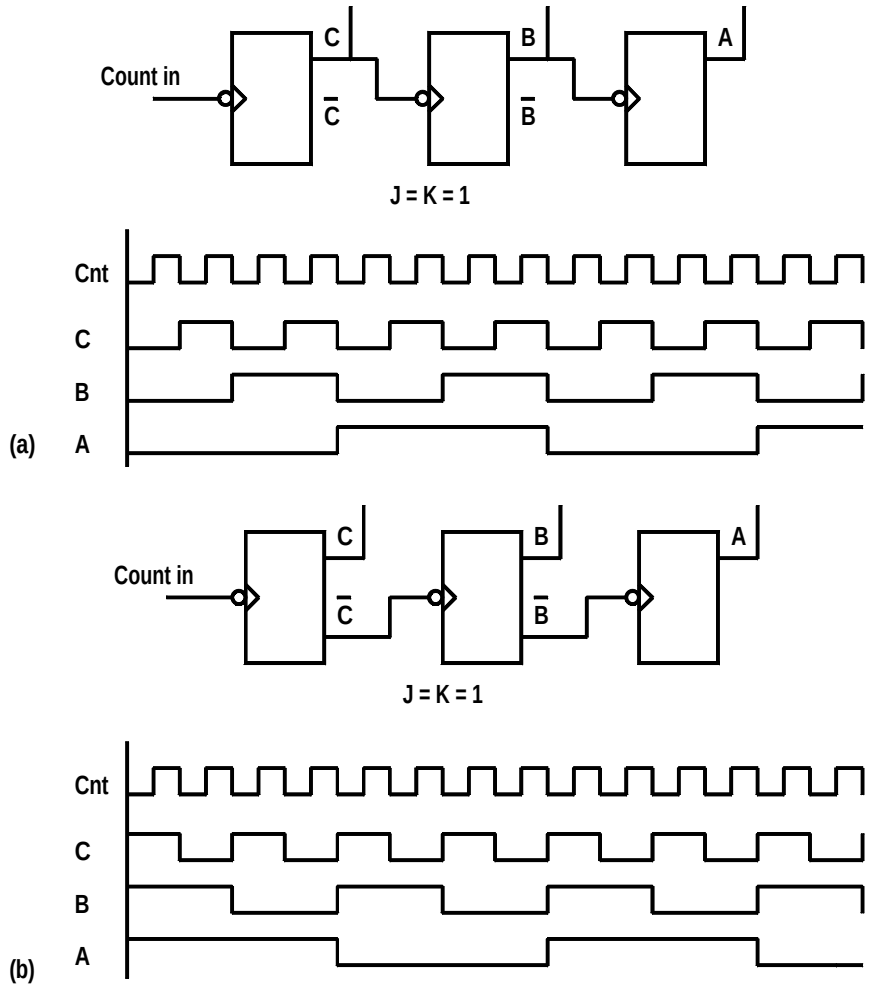

Figure 24.2: (a) 3 bit up counter. (b) 3 bit down counter.

The counters which we have examined so far all operate in a ripple through mode, that is the count is propagated from one binary stage through to the next stage. This means that each of the binary stages in a counter change state on a count change from 1111 to 0000 at slightly different times and the times are determined by the propagation time through a single stage. These counters are therefore termed **asynchronous counters**. This has two serious consequences. The first is that there is a limitation on the speed of response of the counters which manifests itself in an upper frequency limit to the count rate. The second and more serious limitation is that any read out circuit which reads all of the output bits simultaneously will give an incorrect reading if the output is read while a count transition is propagating through

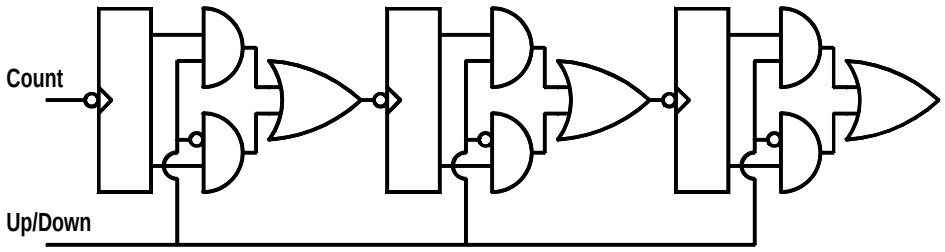

Figure 24.3: Switchable 3 bit up/down counter.

the counter. Therefore any readings from an asynchronous counter which are made "on the fly" cannot be used for control purposes such as batch counting or fringe counting in numerically controlled machines.

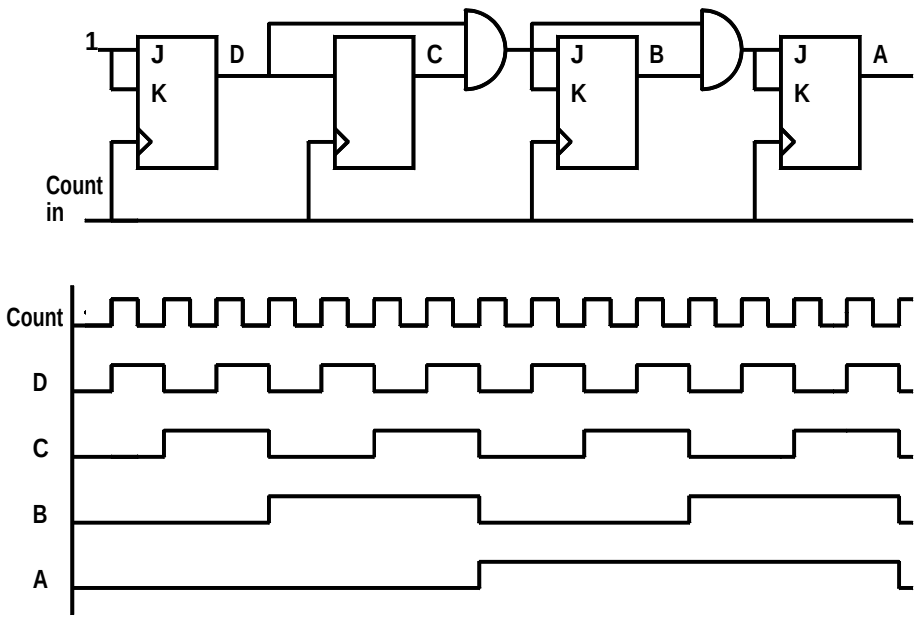

Figure 24.4: Synchronous counter and counting waveforms.

A synchronous counter in which all of the outputs change state simultaneously avoids these readout problems at the expense of increased circuit complexity. The basic design aim for such a counter is that all of the stages should change state simultaneously. This implies that the incoming count pulse must be fed to all binary counter stages simultaneously or in parallel and that a binary stage must change state only if the preceding stages are in

a state which requires a toggle or count to be registered by that stage. This increased complexity of logic gating between binary stages of the counter can be seen in the logic gate circuit for the synchronous counter shown in Figure 24.4.

The logical principle is that stage $n+1$ of this binary counter should only change state at a positive clock edge when the logical AND of the outputs of the previous n stages is a logic 1. This can easily be verified by examining the natural sequence of the first 16 binary numbers shown in the table in Unit 6, page 33. This is implemented in Figure 24.4 in the form of serial logic using the equivalence:

$$X.\text{AND.}(Y.\text{AND.}(Z)) = X.\text{AND.}Y\text{AND.}Z$$

The logical AND of the outputs of the lower order binary counters is applied to the J and K inputs to the JK flip flops and the toggling action of a flip flop is inhibited unless the logical AND of the lower order binary counters is a logic 1 which puts the JK flip flop in the $J = K = 1$ or toggling mode..

24.1 Problems

24.1 Draw the timing diagram showing the count input and the four outputs from the modulo 10 or decade counter shown in Figure 24.1 for 15 count input cycles.

24.2 Draw the logic gate circuit for the NAND gate reset for a modulo 13 counter which uses a circuit similar to that in Figure 24.1.

24.3 An up/down counter has a switch which allows the counter to be operated either as an up counter, with the transfer connections coming from the Q outputs or as a down counter with the transfer connections coming from the $\overline{Q}$ outputs. Design an AND/OR gate circuit which will allow the signals to be taken from either source under the control of a single u/d signal line. Specify the properties of the AND/OR gate circuit in a function table.

24.4 What modifications could be made to the circuit shown in Figure 24.1 so as to avoid the need for inverters at the input to the NAND gate which detects the count of 10?

24.5 Modify the circuit shown in Figure 24.1 so as to implement a base 12 or Modulo 12 counter.

24.6 A BCD (Binary Coded Decimal) counter has four outputs A, B, C and D, representing the four bits of the binary numbers from 0000 to 1001. A led (light emitting diode) lights when current flows through the diode when it is forward biased. A seven segment display contains seven leds arranged in the pattern shown in Figure 24.7 and labeled a, b, c, d, e, f, g as shown. In a common anode seven segment display the anodes of the diodes are connected together. A particular segment of the display is driven from the output of a NOR gate and lights when the NOR gate is at logic 0. The inputs to an AND/NOR gate array are the A, B, C, D signals from the BCD counter or their inverses. Prepare a truth table for the AND/NOR gate array which four inputs A, B, C, D from the BCD counter and which has seven outputs for each of the seven segments and which will cause the appropriate decimal digit to be displayed on the seven segment display.

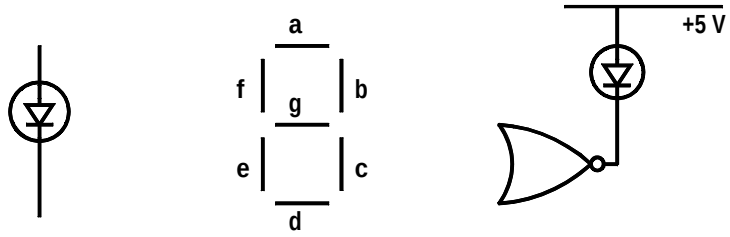

Figure 24.5: BCD to seven segment display driver.