Unit 23 JK flip flop

- In a JK flip flop the indeterminate output state is replaced by a toggled output.
- The Master-Slave flip flop avoids racing by splitting the read-in operation and read-out operations into two separate operations which occur on opposite edges of the clock pulse.
- When J = K = 1, a JK flip flop will operate as a single stage binary counter.

In Unit 22 we showed that passing a square clock signal through a CR differentiator gave a short positive pulse which can be used as a positive edge trigger or gate for flip-flops. In pratice, edge triggering is implemented by using the time delay which occurs between a signal being applied at the input of an inverter and the inverted signal appearing at the output. This propagation delay time is typically between 10 and 20 ns depending on the integrated circuit fabrication technology.

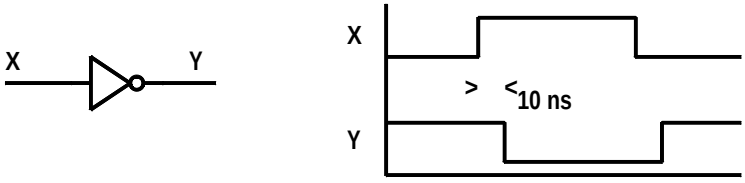

Figure 23.1: Timing waveforms for inverter

This delay in the inverter can be used to generate a short 10 ns pulse coincident with the positive going edge of a square waveform by using the circuit shown in Figure 23.2. There is a 10 ns time delay between the arrival of the positive going edge at the input and the emergence of the inverted negative going output edge during which both the input and output of the inverter are at logic 1. This gives a logic 1 output from the AND gate which lasts for 10 ns. Note, however, that the output from the AND gate is itself delayed in propagating through the AND gate as shown in the timing diagram. Also there is no positive pulse associated with the negative going edge of the input signal and this circuit therefore acts as a positive edge gate.

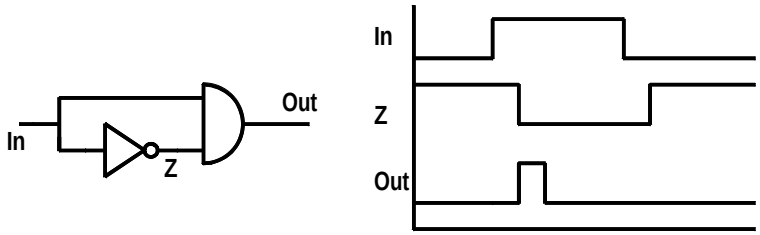

Figure 23.2: Positive Edge Trigger Timing Waveforms

Therefore, an edge trigggered flip-flop is really a level triggered flip-flop with an internally generated very short gate. It is also important that the other signals to the flip-flop do not change during this short gate time otherwise the results may not be fully predictable. It is also a requirement that the rising edge of the trigger waveform make the positive going transition in a time shorter than this internally generated gate otherwise the 10 ns square gate may not be successfully generated.

The RS and D type flip flops already described in Unit 22 perform essentially one function—they latch and store a memory of the logic state presented at the input. The devices do not carry out any computational function. If we now introduce another layer of feedback from the output of an RS flip flop back to a clocked input and use the propagation delays within the circuit, we obtain a JK flip flop and a fundamental change in operation which allows counting and other computational functions. A circuit for a JK flip flop is shown in Figure 23.3.

We have used the NAND gate version of the $\overline{RS}$ flip-flop and repeat the function table for this device again for convenience.

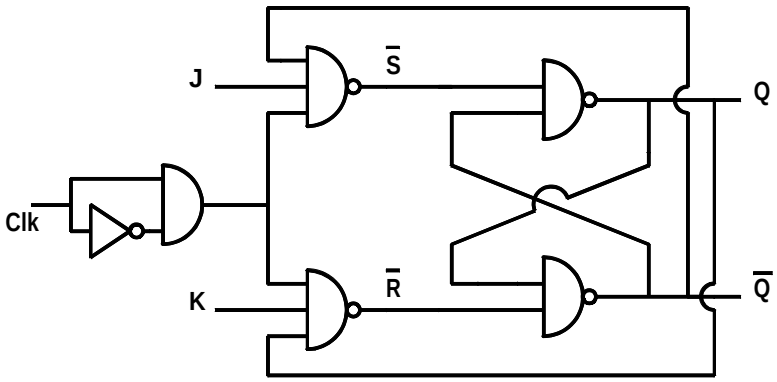

Figure 23.3: JK flip flop schematic circuit.

$\overline{R}$	$\overline{S}$	Q	$\overline{Q}$
1	1	Q_{Old}	$\overline{Q}_{Old}$
1	0	1	0
0	1	0	1
0	0	?	?

Function Table for RS Flip-Flop

Clk	J	K	Q_{Old}	$\overline{R}$	$\overline{S}$	Q_{New}	Comments
0	X	X	X	1	1	Q_{Old}	No change
↑	0	0	X	1	1	Q_{Old}	No change
↑	0	1	0	1	1	0	Q follows J
↑	0	1	1	0	1	0	Q follows J
↑	1	0	0	1	0	1	Q follows J
↑	1	0	1	1	1	1	Q follows J
↑	1	1	0	1	0	1	Toggles
↑	1	1	1	0	1	0	Toggles

Function Table for J-K Flip-Flop

We analyse the operation of this JK flip-flop by examing what happens when we apply, in turn, all possible combinations of signals to the Clock and the J and K inputs for each of the two possible present states of the JK output. These are the conditions defined by the first four columns in the function table. The analysis consists of examining the inputs to each of the two NAND gates and computing the corresponding $\overline{R}$ and $\overline{S}$ inputs. The resulting outputs from the $\overline{R}$ and $\overline{S}$ give the new Q and $\overline{Q}$ outputs.

In the last two lines of the function table where we get toggling action or change over action, we can see why the JK flip-flop must be an edge triggered device. The positive going edge generates the short time duration positive gate which allows the RS flip-flop to be triggered into changing state but which reverts to a logic 0 before the changed Q and $\overline{Q}$ can propagate back and cause another trigger. The edge trigger action prevents this "racing" phenomenon. This has phenomenon already been encountered in the ring of three inverters in Figure 22.2 which shows how this "racing" oscillation can occur.

Rules for the operation of the Positive Edge triggered JK flip-flop:

1. Nothing changes in the absence of a positive edge on clock input.

2. When a positive clock edge occurs:

   (a) If J = 0 and K = 0 then there is no change

   (b) If J = 1 and K = 0 then Q $\rightarrow$ 1

   (c) If J = 0 and K = 1 then Q $\rightarrow$ 0

   (d) If J = 1 and K = 1 then Q toggles (1 $\rightarrow$ 0 or 0 $\rightarrow$ 1)

The novel and distinctive feature of the JK flip flop, called **toggling action** which occurs when $J = 1$ and $K = 1$ and a positive going clock input edge causes a cross transfer of outputs so that for instance, if the old value of the Q output was $Q_0 = 1$, then on a clock pulse, the output is driven to the $Q = 0$ output state. Similarly if the Q output was at $Q_0 = 0$ then a clock input will cause the Q output to go to the $Q = 1$ output state. This toggling action depend essentially on the existence of a propagation delay in the feedback path which allows the old outputs Q and $\overline{Q}$ to determine the transfers of signal at the clock edge.

It would seem that the function table for the JK flip flop contains no ambiguous states but this is not the case. The ambiguity is associated with the implementation of edge triggering. As we have seen, an edge trigger is really a short duration pulse which is applied to the NAND gates at the positive or negative going transition. The effect is a level type gate of short and finite duration. Consider what happens if a logic 1 is applied to a point in the circuit just after the inverter/AND gate Positive Edge Trigger in Figure 23.3. When $J = K = 1$ and the clock level is 1 then a $Q = 1$ output gives a logic 1 output from the lower NAND gate which gives a logic 0 at the $\overline{R}$ input which drives the Q output to a $Q = 0$ state and the $\overline{Q}$ to a $\overline{Q} = 1$ state which allows a logic 0 at the $\overline{S}$ input which drives the Q output back to a $Q = 1$ state. The Q output therefore changes state rapidly at a rate which is equal

to twice the signal propagation time around the loop. The system is said to **race** as a result of repeated toggling. This race occurs when the duration of the effective edge triggered clock level is greater than the propagation time around the circuit and it is evident that this is not a desirable mode of circuit operation.

The racing problem is avoided by using two flip flops in a Master-Slave configuration as shown in Figure 23.4.

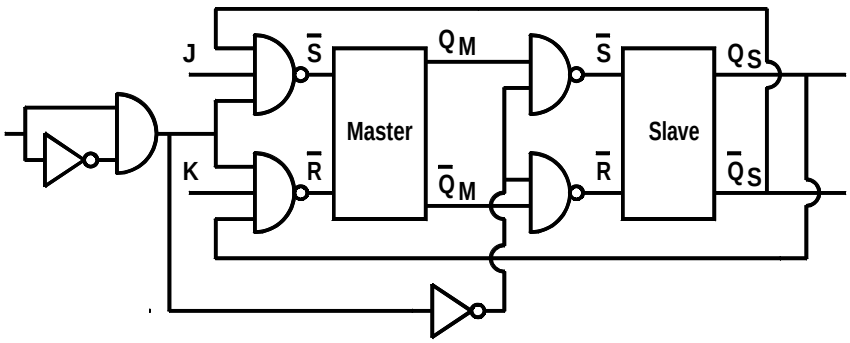

Figure 23.4: Master-Slave JK flip flop.

When $J = K = 1$, a positive clock edge causes an initial $Q_S = 1$ output to give a 1 at the R input of the Master flip flop which causes the Q_M output to be driven to a logic state $Q_M = 0$ and $\overline{Q_M} = 1$. At the next negative clock edge the $\overline{Q_M} = 1$ appears at the R input to the slave flip flop and the Q_S output therefore goes to the state $Q_S = 0$. Toggling action has now taken place without any possibility of racing since the transfer between the input and output is a two stage process which requires both positive and negative clock edges.

A similar analysis for an initial $Q_S = 0$ state also shows that toggling action takes place for this initial state.

The distinctive application of the JK flip flop is illustrated in Figure 23.5. In this application the J and K inputs are $J = K = 1$ and clock pulses are applied to the Clk input. These clock pulses are usually a train of equally spaced pulses but they do not have to be so. In this example we consider a train of irregularly spaced pulses and a positive edge triggering type of Master Slave JK flip flop.

On the first positive clock edge the $J = K = 1$ is read into the master part of the JK flip flop causing it to toggle from a $Q_M = 0$ to a $Q_M = 1$ state and is stored there. On the negative clock edge, the $Q_M = 1$ of the master JK flip flop is transferred to the slave JK flip flop and appears at the Q output as a $Q = 1$ output. On the next positive clock edge the master flip

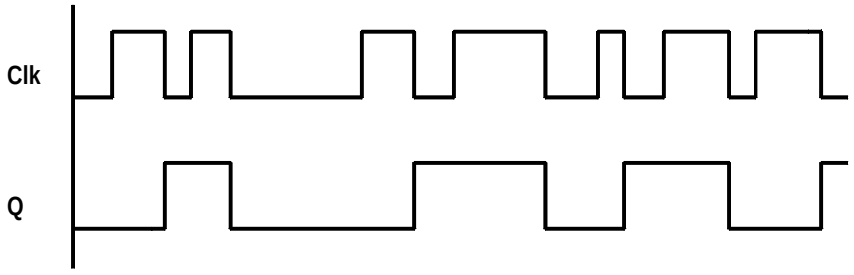

Figure 23.5: Timing diagram for a Master Slave JK Flip Flop with $J = K = 1$

flop toggles again and on the subsequent negative clock edge, the new master value is transferred to the output again and the output returns to $Q = 0$. Thus two full cycles of the clock are required to cause the output to show one full cycle of $Q = 0$ to $Q = 1$ followed by a return to $Q = 0$. The frequency of the clock waveform is therefore divided by a factor of 2. Or alternatively, we have made a single stage binary counter.

If four master slave JK flip flops are connected together so that the output of one is connected to the clock input of the next, we can make a multistage binary counter as shown in Figure 23.6.

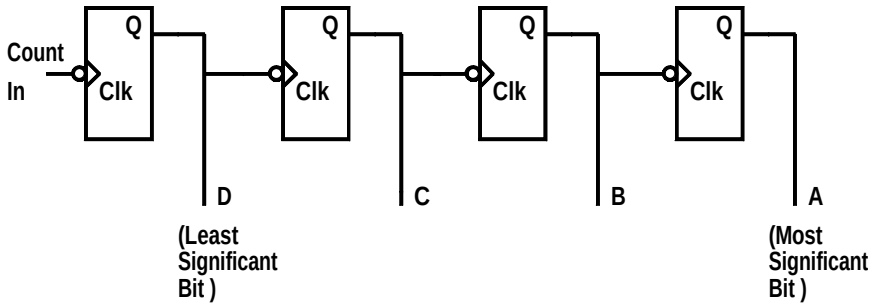

Figure 23.6: Counter configuration. $J = K = 1$ (not shown).

If we assume that all of the flip flops are initialized to the $Q = 0$ output state, then this daisy chained configuration forms a four bit binary counter where the count Z is given by $Z = ABCD$ where A represents the most significant bit, D the least significant bit and where Z is the number of full cycles of the input stream.

If a stream of input signals is applied at the input then the waveforms which would be observed on a 5 channel oscilloscope would be as shown in Figure 23.7. We have also added in, at the bottom, the binary value of the count, Z. It should also be noted that after $2^4 = 16$ full clock cycles at the

input, this 4 bit binary counter has wrapped around to give a $Z = 0000$ output.

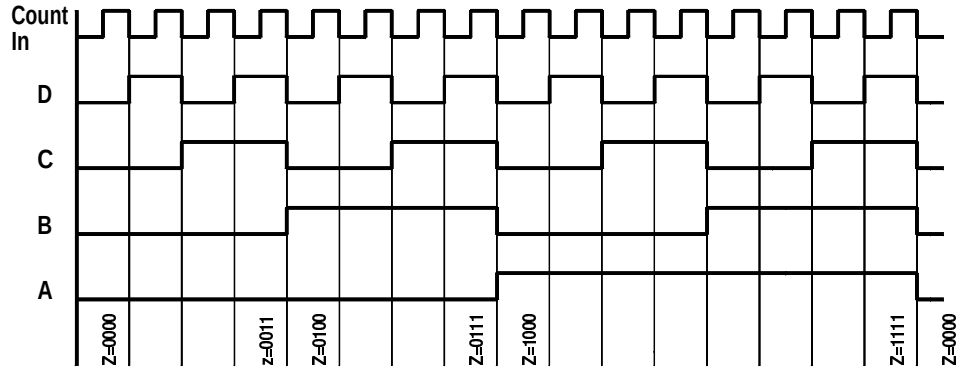

Figure 23.7:

23.1 Problems

23.1 How can the circuit shown in Figure 23.2 be modified so as to implement a negative edge triggered gate?

23.2 Trace through the changes which occur in the master slave JK flip flop for inputs of $J = K = 1$ and for an initial state of $Q_S = 0$ and show that the final state after a positive going clock edge followed by a negative going clock edge is an output state $Q_S = 1$.

23.3 What would be the output waveform in Figure 23.6 if a JK flip flop were used instead of a Master slave JK flip flop?

23.4 Redraw the output waveform which would be obtained if the JK flip flop in Figure 23.6 had an initial $Q = 1$ output state.

23.5 Fill in the missing values of the binary count, Z, at the bottom of Figure 23.7.

23.6 Look up the TTL Data book from Texas Instruments and enumerate the available versions of JK Flip-Flops together with the type numbers and differences.

23.7 Look up the CMOS Fata Book and enumerate the various types of JK Flip-Flops which are available.