# Unit 22 RS and D type Flip-Flops

- Feedback circuits such as flip flops are analyzed by cutting the feedback loop and applying signals to the open circuit.
- A flip flop is stable in either of two states.
- A RS flip flop can be switched between stable states by application of a Reset or Set input.
- D type flip flops use an inverter at the input to prevent the occurrence of an indeterminate state.
- Gated flip flops can only make transitions when a gate or clock pulse is present or at the positive or negative going edge of a clock pulse.

The Boolean and other logic circuits which we have considered in Units 9 to 21 operate as static circuits, independently of time. The outputs are determined only by the state of the static inputs. We now introduce an extra feature to the circuit—we introduce feedback from the output back to an input so that the circuit state is now specified not only by the $n$ primary inputs but also by one or more of the outputs from the circuit.

There is a very powerful analysis method which can be used in determining the performance of logic circuits in which signal feedback is used. It is based on the reasonable rule that a signal cannot be both a logic 1 and a logic 0 at the same time. So if the feedback path is cut and an external signal applied at the cut then, when the signal is traced on around the circuit to arrive at the other side of the cut, the only stable states for the circuit will be the states when the two signals on each side of the cut are the same.

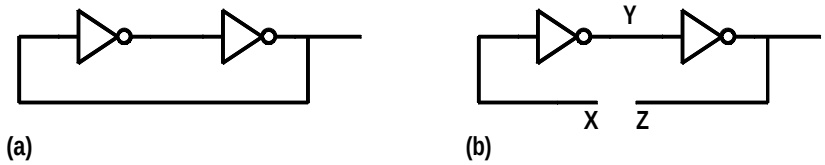



Figure 22.1: NOT gate feedback latch circuit.

As an application of this analysis method we consider the simple two inverter NOT circuit shown in Figure 22.1 (a). The analysis consists of cutting the circuit as shown in Figure 22.1 (b) and applying an external signal at the point X. The possible values of the input signal, X, intermediate signal, Y, and resulting output and feedback signal, Z, are shown in the table.

| X | Y | Z |
|---|---|---|
| 0 | 1 | 0 |
| 1 | 0 | 1 |

It is easily seen that for both input signals 0 and 1, the outputs are a matching 0 and 1 and that the signals across the cut match. Therefore there will be no change to the circuit if a connection is made across the cut. This is therefore a circuit which is stable in either state.

One difficulty is that there is no method of changing the state of the circuit. The circuit state can be changed if the NOT gates are replaced by NAND (or NOR) gates as shown in Figure 22.2

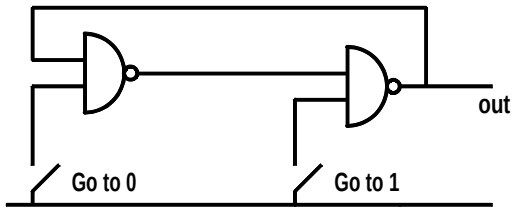



Figure 22.2:

There are two external inputs to this circuit. When the left hand input is brought to a logic 0 from the default logic 1 the circuit output is driven to a logic 0 and remains at a logic 0 after the input is released back to a logic 1. When the right hand input is brought to a logic 0 from the default logic 1 the output is driven to a logic 1 and remains at a logic 1 after the input is released back to a logic 1. This latching circuit therefore retains a memory of the state to which it was last driven and remains in that state. A good analogy is a light switch which remains either ON or OFF depending on the last operation of the light switch. It is also worth noting that turning ON a latch or switch that is already ON has no effect. Similarly turning OFF a latch or switch that is already OFF also has no effect.

The power of this consistency analysis method is revealed when the three inverter NOT gate circuit, shown in Figure 22.3, is analyzed.

When the feedback loop is cut and the input signal is compared with the feedback signal, this truth table is obtained.

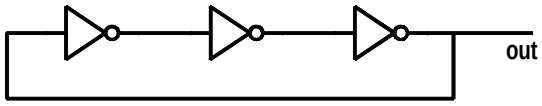



Figure 22.3:

| In | Out |
|---|---|
| 0 | 1 |
| 1 | 0 |

The logic signals at each side of the cut are inconsistent so the circuit will not be stable. Instead of being stable in one state the circuit oscillates with a periodic time, $T$, which is six times the signal propagation delay in each of the inverter NOT gates.

Consider the circuit in Figure 22.4 (a) which is redrawn in Figure 22.4 (b).

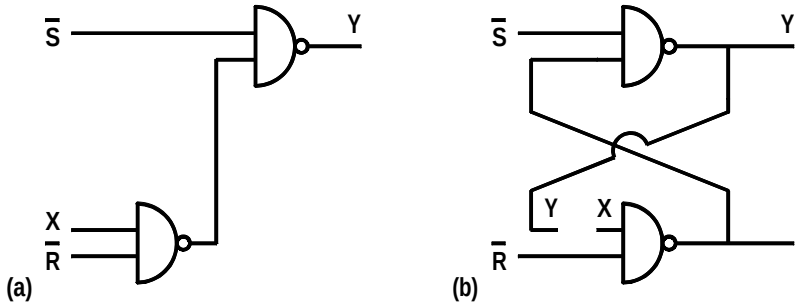


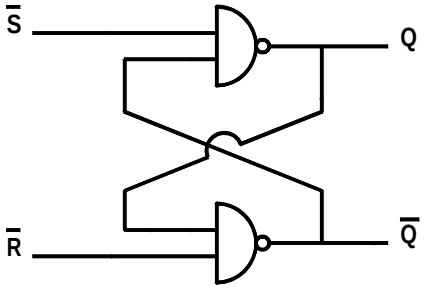

Figure 22.4: NAND gate version of RS flip flop (Active LOW).

The circuit in Figure 22.4 (a) has three inputs: $\overline{S}$ (set), $\overline{R}$ (reset) and X and a single output, Y. When the circuit is redrawn with the **same** connections as shown in Figure 22.4 (b), which emphasizes the symmetry of the circuit, the effect of making a connection between X and Y can be examined. If the logic values at X and Y are the same then there should be no effect or change when X is connected to Y. If the signal at X is not the same as the signal at Y then connecting X to Y will cause changes to the circuit state. So we prepare a truth table which shows all the possible combinations of the inputs $\overline{R}$, $\overline{S}$ and X and the dependent output Y. Valid or stable circuit states are those indicated in the truth table where (by DeMorgan):

$$Y = \overline{\overline{\overline{X}.\overline{R}.\overline{S}}} = \overline{\overline{X}.\overline{R}} + \overline{\overline{S}} = X.\overline{R} + \overline{\overline{S}}$$

| $\overline{R}$ | $\overline{S}$ | X | Y | X = Y ? |
|---|---|---|---|---|
| 0 | 0 | 0 | 1 | Unstable |
| 0 | 1 | 0 | 0 | Stable |
| 1 | 0 | 0 | 1 | Unstable |
| 1 | 1 | 0 | 0 | Stable |
| 0 | 0 | 1 | 1 | Stable |
| 0 | 1 | 1 | 0 | Unstable |
| 1 | 0 | 1 | 1 | Stable |
| 1 | 1 | 1 | 1 | Stable |

When the connections between X and Y are made the NAND gate version of the RS flip flop is as shown in Figure 22.5 and the truth table is also shown. The convention is that the outputs are $Q$ and $\overline{Q}$ signifying that the two outputs are usually opposite to each other except for the disallowed input combination of $\overline{S} = 0$ and $\overline{R} = 0$. This combination is not really disallowed. It is an input combination which forces both the $Q$ and $\overline{Q}$ outputs to logic 1. However, the state when the inputs are removed is not fully predictable as it depends on which input was changed first.



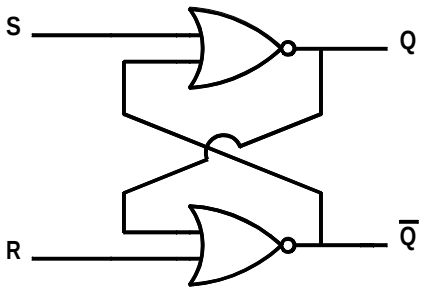

| $\overline{R}$ | $\overline{S}$ | Q | $\overline{Q}$ |
|---|---|---|---|
| 1 | 1 | Q | $\overline{Q}$ |
| 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 |
| 0 | 0 | ? | ? |

Figure 22.5: NAND gate version of RS flip flop (Active LOW).

The RS flip flop can also be constructed from elemental NOR gates as is shown in Figure 22.6. The truth table is slightly different in this case as the indeterminate state now occurs for inputs of $R = 1$ and $S = 1$ and the latched state occurs for inputs of $R = 0$ and $S = 0$

Note that the truth table outputs, $Q$ and $\overline{Q}$, for a NOR RS flip flop are opposite to those for the NAND RS flip flop. Both types of flip flop are used but the NOR gate version is the more common.

There are two significant problems associated with the use of the RS flip flop; there is the indeterminate state output and also there is no facility for synchronizing the circuit transitions with other transitions in a circuit.




| R | S | Q | $\overline{Q}$ |
|---|---|---|---|
| 1 | 1 | ? | ? |
| 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 |
| 0 | 0 | Q | $\overline{Q}$ |

Figure 22.6: NOR gate version of the RS flip flop (Active HIGH).

The indeterminate output state is avoided by preventing the input combination causing the problem from ever appearing at the inputs. This is done by including an inverter at the input as shown in the circuit for the D type flip flop in Figure 22.7. A single D input is inverted and the inverted and noninverted signal applied to the $\overline{R}$ and $\overline{S}$ inputs. Therefore the $\overline{R}$ and $\overline{S}$ inputs can never be the same and the only signal combinations that can be applied to the flip flop are those in the two central rows of the RS flip flop truth tables shown in Figures 22.5 or 22.6.

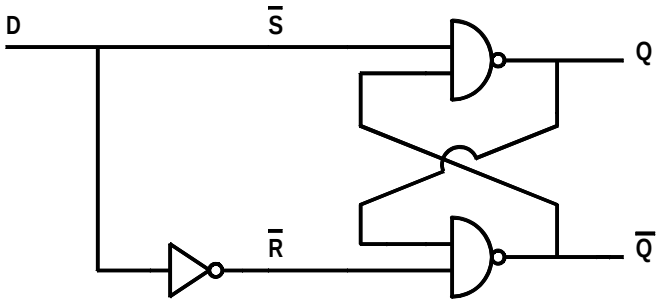



Figure 22.7: D type flip flop.

The second problem, the synchronization prblem, is solved by introducing a clock synchronization waveform to the circuit and requiring that state transitions in the circuit only occur when the clock is in its logic 1 part of its cycle. This is shown in the Gated D type flip flop shown in Figure 22.8.

The truth table which describes the transitions is also shown. An entry of $Q$ in the column for $Q$ means that the value of $Q$ from before the clock transition is the value which is obtained in the circuit. An input shown as an $X$ means that the logic state for that input is has no effect.

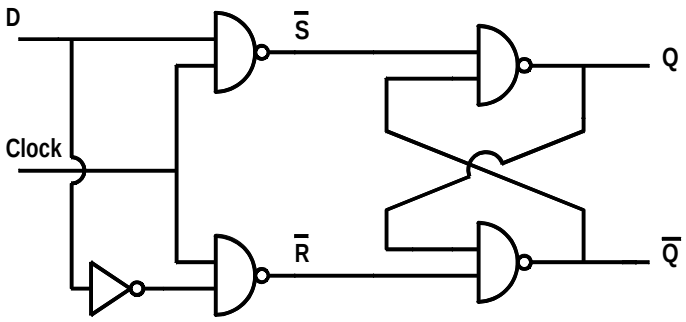



Figure 22.8: Gated D type flip flop.

| Clk | $D$ | $\overline{S}$ | $\overline{R}$ | $Q$ | $\overline{Q}$ |
|---|---|---|---|---|---|
| 0 | $X$ | 1 | 1 | $Q$ | $\overline{Q}$ |
| 1 | 0 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 1 | 0 |

So the rule for this type of gated D type flip flop is that the logic state of the $D$ input is transferred to the $Q$ output while the clock is at logic 1.

If a square waveform is passed through a CR filter circuit, the output will consist of a series of positive and negative pulses or spikes coincident with the edges of the square waveform as shown in Figure 22.9.

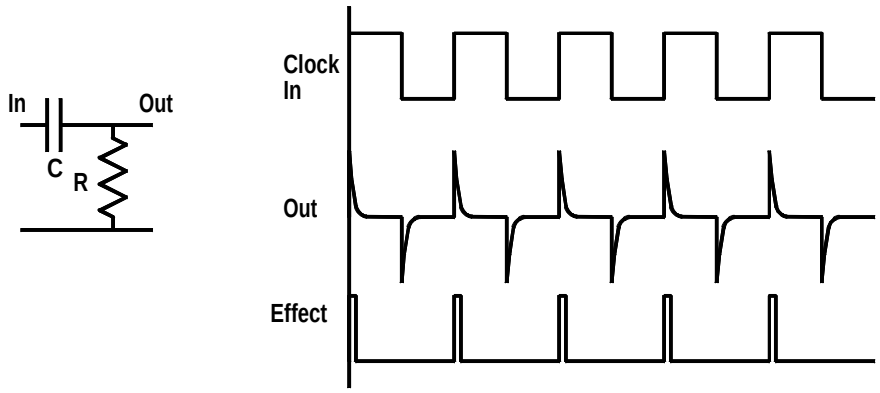



Figure 22.9: Differentiation of a square waveform.

The duration of the spikes will depend on the time constant, $T = RC$, for the CR filter. The negative spike will have no effect on the logic circuit but the positive spike is effectively a fixed duration gate, coincident with the clock edge, during which the gate of the gated flip flop—the two AND

gates—will allow signals to transfer from the $D$ input to the $Q$ and $\overline{Q}$ outputs. Effectively, this gives us a device which takes a snapshot of the D input. This is in contrast to the level triggered D flip flop which we had before. In integrated circuit edge triggered type inputs, the edge detection is carried out using logic circuits with delays rather than the RC filter circuit shown here but the principle of operation is similar. The effects of these two types of gating, level triggered and edge triggered are shown in the timing diagrams in Figure 22.10.

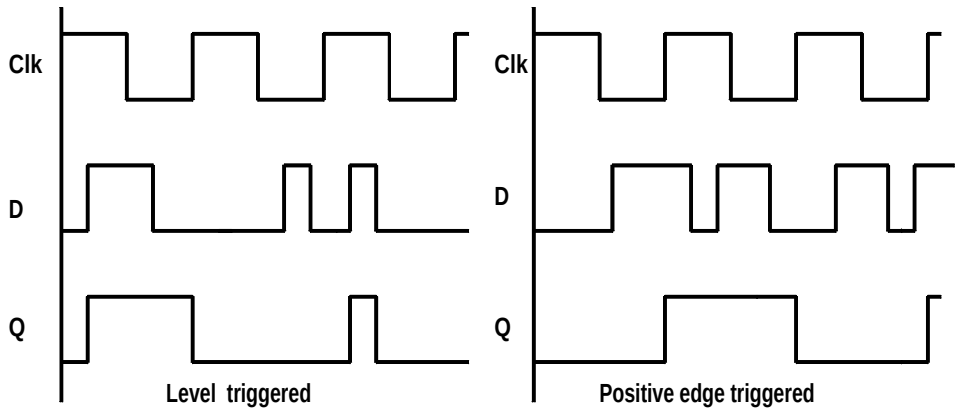



Figure 22.10: Timing waveforms for level and edge triggered D type flip flops.

In order to initiate a sequence of transitions, it is necessary to start with all the flip flops in a known initial condition. Most integrated circuit flip flops, therefore, have Preset and Clear inputs which allow the flip flop to be driven to an initial known condition before any computations starts. We therefore have the conventional representation of flip flops with various features as shown in Figure 22.11.

The edge type clock input is marked by an arrow $>$ inside the function block. The negative edge triggered clock is denoted by the inverting circle $\circ$ and the $>$ symbols

As an example we give the function table for the last of the D type flip flops shown in Figure 22.11 in the form provided by the IC manufacturers, where L = logic 0, H = logic 1 and $\downarrow$ denotes a negative edge transition.

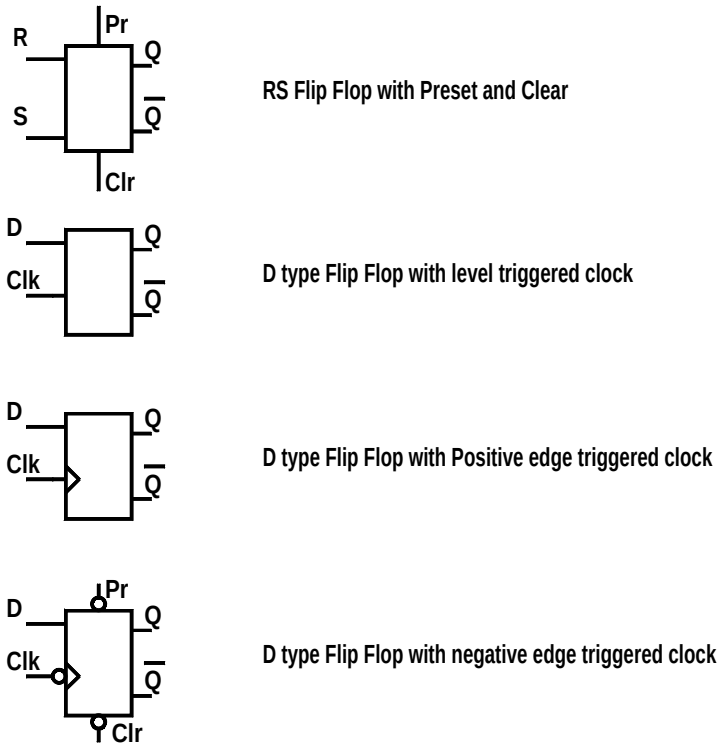



Figure 22.11: Typical circuit schematics for various types of D type flip flops

| Inputs | | | | Outputs | | Comment |
|---|---|---|---|---|---|---|
| Pr | Clr | Clk | D | $Q$ | $\overline{Q}$ | |
| L | H | X | X | H | L | Preset |
| H | L | X | X | L | H | Cleared |
| L | L | X | X | H* | H* | Unstable |
| H | H | $\downarrow$ | H | H | L | Transfer D$\rightarrow$Q |
| H | H | $\downarrow$ | L | L | H | Transfer D$\rightarrow$Q |
| H | H | $\uparrow$ | X | $Q_o$ | $\overline{Q_o}$ | No change |
| H | H | H | X | $Q_o$ | $\overline{Q_o}$ | No change |
| H | H | L | X | $Q_o$ | $\overline{Q_o}$ | No change |

**Truth table for D type flip flop with negative edge triggered clock.**

## 22.1 References

*Texas Instruments TTL Data Book*
Texas instruments (1982)

## 22.2 Problems

22.1 Is there any significant difference between the circuit in Figure 22.2 and the circuit in Figure 22.5?

22.2 Why does the negative going pulse in Figure 22.9 have no effect when it is applied to a logic gate input?

22.3 The clock, active-low Preset and D waveforms shown in Figure 22.12 are applied to the inputs to a positive edge triggered D type flip flop. Sketch the resulting $Q$ and $\overline{Q}$ output waveforms.

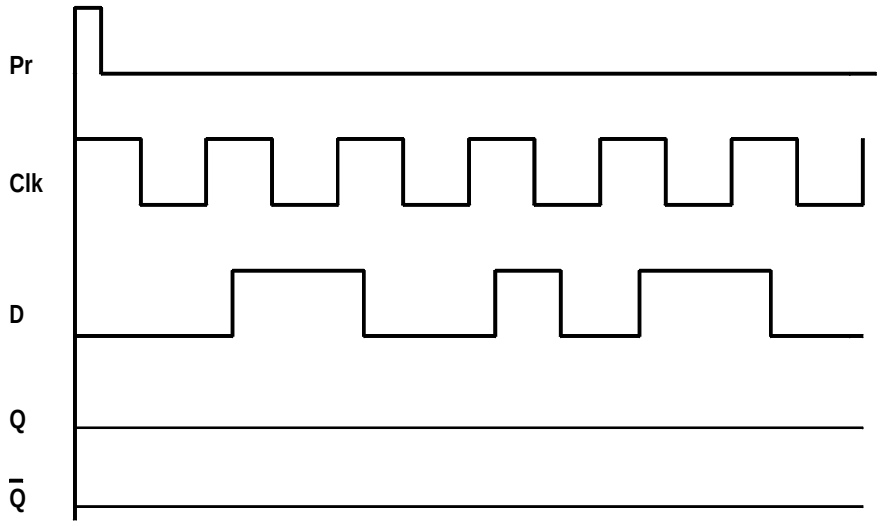



Figure 22.12: