Unit 4 ECL.

- Emitter Coupled Logic (ECL) avoids saturation effects by operating in differential mode with a limited emitter current.
- Total current in transistor pair is less than saturation current for one transistor.
- Unsaturated transistors have a faster switching time because of the absence of minority charge storage.
- ECL logic gates can operate at high switching speeds.

The speed of transistor transistor logic (TTL) circuits is limited by the tendency of common emitter circuits to go into saturation due to injection of minority carriers into the collector region. The minority carriers take a finite time to diffuse out of the collector region after the signal is removed and it is this diffusion time that limits the speed of response of the TTL circuits. The tendency to saturate can be limited by the use of Schottky diodes between the base and collector giving the Schottky TTL devices that we discussed in Unit 2.

An alternative approach is to limit the base current of the transistor so that saturation does not occur but the unavoidably wide spread of the current gain, β or h_{fe} of bipolar transistors makes this approach very difficult to implement in common emitter amplifier type circuits.

Transistors can, however, be prevented from going into saturation by the use of another circuit configuration which balances two nearly identical transistors against each other in a differential mode as shown in Figure 4.1. This takes advantage of the fact that, while it is not easy to fabricate bipolar transistors having a specific value of h_{fe}, it is easy to fabricate transistor pairs having nearly equal h_{fe}. The transistor circuits are connected or coupled together through the emitters rather than from collector to base giving rise to the description of this type of logic as ECL or Emitter Coupled Logic.

The core circuit in this technology is the differential amplifier configuration shown in Figure 4.1.

The input signal is compared with a reference voltage and, depending on the sign of $(V_{in} - V_{ref})$, the output will swing either positive or negative. The

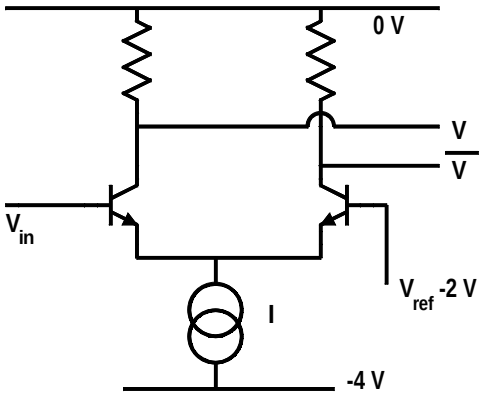

Figure 4.1: Differential mode operation of transistors.

transistors are prevented from going into saturation because the constant current supply to the emitters is set at a value less than the saturation current for a single transistor. The operating point is then restricted to the unsaturated part of the load line and cannot reach the saturation point, Q, which is indicated in Figure 4.2 and which was discussed in Unit 2.

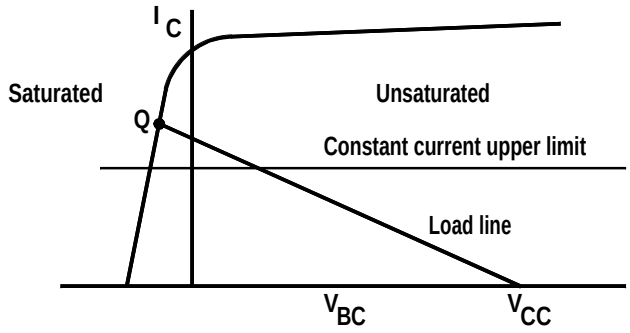

Figure 4.2: Constant current source restricts the operating point to values less than the saturation current.

The reference voltage in the circuit in Figure 4.1 is chosen so that the output voltage changes on the two collectors are symmetric and opposite which gives either inverting or noninverting operation and also allows us to mark the two outputs as V_{out} and $\overline{V_{out}}$ as shown in the diagram.

When the input voltage is equal to the reference voltage the circuit is balanced. Since the input stage is also an amplifier stage, a small change of the input voltage, of the order of 125 mV, is sufficient to cause essentially all of the current to flow through one or other of the two collectors. The minimum

peak to peak voltage swing required for switching is therefore 250 mV but in practice 750 mV is used to provide good noise immunity.

A point worth noting is that this type of differential amplifier usually requires the use of dual power supplies and also that the supply voltages are different from the +5 V used in TTL and CMOS. For instance the F100K ECL digital family from National Semiconductors use negative voltage power supplies of -5.2 V and -2.0 V which are very different from the usual TTL or CMOS supplies. However, the ECL devices are used in very fast computing applications and are not mixed with TTL or CMOS so power supply compatibility problems do not usually arise.

Implementation of the OR and NOR function is shown in Figure 4.3. In this circuit, we introduce buffering of the output by means of the emitter followers connected to the collector resistors. The emitters are open and will act as line drivers with the input resistors to the negative supply acting as emitter loads.

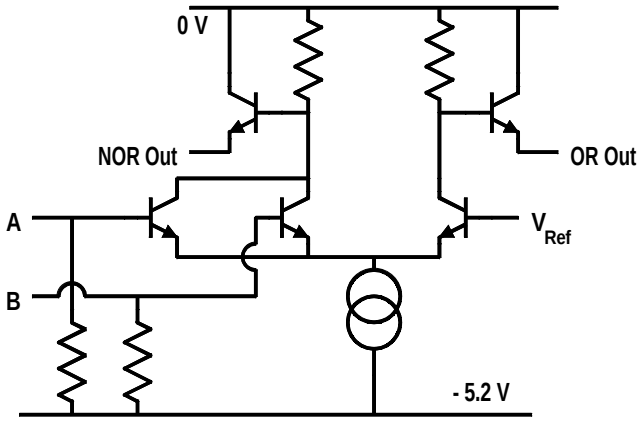

Figure 4.3: ECL OR / NOR gate implementation.

The AND and the NAND gate can be implemented by wiring the differential amplifiers in series as is shown in Figure 4.4.

It is to be noted that the ECL circuits described utilize negative power supplies which are not always available and are not compatible with the +5 V supplies used in ttl and CMOS circuits. For this reason a slightly different version of ECL called positive ECL or PECL has been developed which run off +5 V supplies. There are also interface or translator ICs available which translate the signal voltage levels of ttl and CMOS to those of PECL and vice versa which allow the construction of mixed circuits which take advantage of the benefits of each technology.

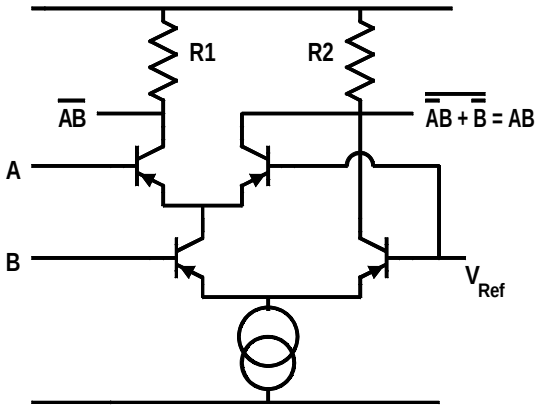

Figure 4.4: ECL AND / NAND gate implementation.

One of the features of ECL and PECL technology is that the output impedance is 50 Ω so that the output signal can be coupled into 50 Ω transmission line and distributed to other parts of the circuit board or to other pieces of equipment. The only requirement is that the transmission line be properly terminated with a matching 50 Ω resistance so that there are no signal reflections from the end of the line.

The applications of ECL are in high speed digital signal processing. For instance in the case of a video display having the moderate resolutionof 1000 by 800 pixels and refreshed ar 50 Hz the pixel rate is 40 MHz without taking into account the 8 bits of resolution per pixel so high speed requirements can arise in surprisingly mundane applications.

4.1 References

National Semiconductors, *F100K ECL 300 series Databook and Design Guide*

Mauro, R., (1989) *Engineering Electronics: A Practical Approach* Prentice Hall.