Unit 3 CMOS.

Complementary Metal Oxide Silicon.

- Uses complementary MOSFETs.
- Voltage controlled devices.
- Low power.

The key component in CMOS (Complementary Metal Oxide Silicon) digital electronic integrated circuits is the enhancement mode metal oxide field effect transistor which can be fabricated in complementary n channel and p channel forms.

The basic structure of the n channel version of this type of FET is shown in Figure 3.1 and consists of two heavily doped n^+ regions or wells in p type which form the source and drain. The n^+ facilitates the formation of ohmic contacts as we saw in Unit 2.

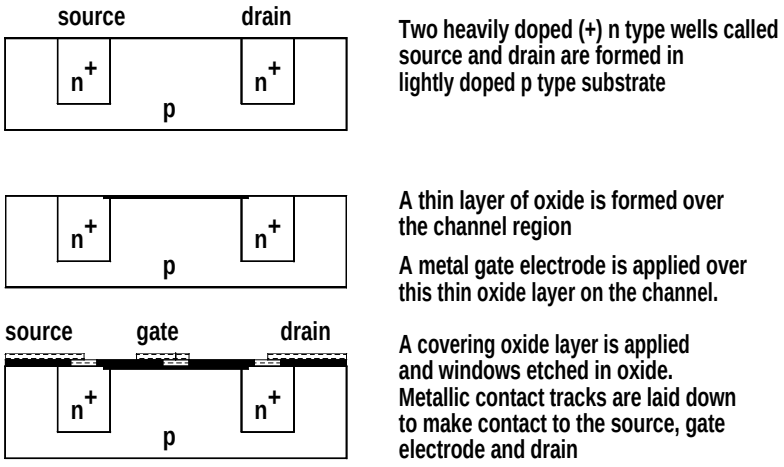

Figure 3.1: Structure of enhancement mode n channel MOSFET.

The region between the source and drain is p type and, as a result, there is no conduction channel between the source and drain when the drain is at a positive voltage with respect to the source. So initially no current flows from the source to the drain. The region between the source and drain is covered with a highly insulating SiO_2 layer which is usually about 0.2 micron thick. A metal gate region is formed over this insulating layer which extends the full width of the gap between the source and the drain but is fully insulated form the source and drain by the SiO_2 layer.

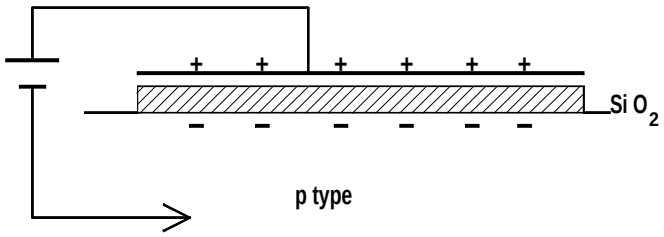

Figure 3.2: Charge layers associated with MOSFET channel enhancement.

This gate electrode and the p type substrate form a capacitor with the SiO_2 acting as the dielectric. When a positive voltage is applied to the gate, relative to the substrate, a positive charge accumulates on the gate and a negative charge layer forms in the p type substrate under the gate. The n type carrier concentration increases and the p type carrier concentration decreases in agreement with the semiconductor equation, $[n][p] = [n_i]^2 = constant$ where $[n]$ and $[p]$ are the respective carrier concentrations and $[n_i]$ is the carrier concentration in intrinsic silicon.

When the voltage applied to the gate electrode exceeds a threshold voltage, V_{Th}, this results in the formation or enhancement of an n type channel between the source and the drain so that current can now flow between the source and drain. The saturation current which flows depends on the gate to source voltage, V_{GS}, the threshold voltage for the formation of the channel, V_{Th}, and the size of the transistor which is a constant for a particular device. This then gives a set of characteristic curves for the enhancement mode MOSFET as shown in Figure 3.3.

The key feature of this device is that a threshold gate to source voltage is necessary for current to flow between the source and the drain and that the gate is insulated by the layer of SiO_2 and therefore it is the gate voltage alone which controls the flow of current. No gate current flows in this type of device except for the very small current which is necessary to change the

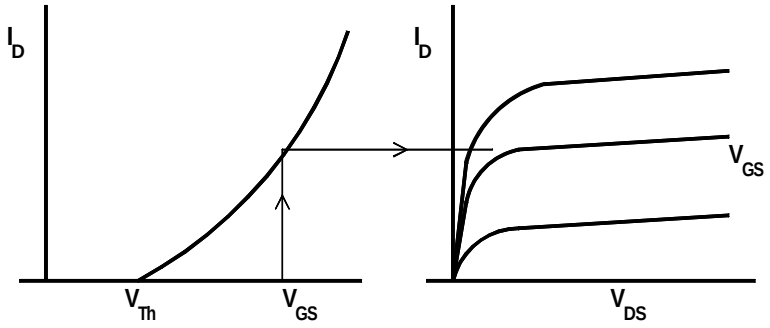

Figure 3.3: Enhancement mode MOSFET characteristic curves.

voltage across the gate to channel capacitance and which is of the order of $1\,\text{pF} \times 5\,\text{V} = 5 \times 10^{-12}\,\text{C}$ per turn on or turn off operation.

From the point of view of digital electronics this device is ideal since it has an inbuilt thresholding function associated with the formation of the enhancement layer.

One of the simplest circuits which uses this MOSFET is the inverter circuit shown in Figure 3.4.

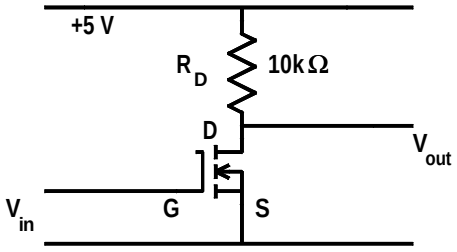

Figure 3.4: MOSFET inverter.

The direction of the arrow on the source to substrate connection shows that this is an n channel device. The channel is shown as three separate heavy segments. The separation of the segments indicates that this is an enhancement type device in which a conductive channel is formed by the application of a voltage to the gate. The gate is shown as an electrode which is isolated from the channel.

In this simple circuit, the output voltage will be at +5 V for gate voltages between 0 V and the gate threshold voltage, V_{Th}, since there will then be no current through the FET and therefore no voltage drop across the 10 kΩ

drain resistor. This also has the consequence that any noise generated within a stage is absorbed at the next stage because the noise noltage is unlikely to exceed the threshold voltage of the enhancement mode FET and therefore will not cause any spurious switching of the FET.

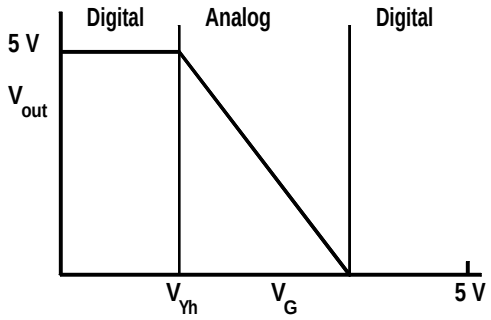

Figure 3.5: Switching characteristic of MOSFET inverter.

As the gate voltage is increased, the threshold voltage is reached and drain current starts to flow. The voltage drop across R_D increases and the drain voltage which is also the output voltage drops as shown in Figure 3.5. There is therefore a region just above the V_{Th} where the output voltage decreases as the gate voltage increases. This is the region where we would use the device if we were working with analog signals. However, here we are interested in digital signals where we only have ON and OFF signals so we operate the circuit so that it it is normally in one or other of the two digital regions and makes as rapid a transition from one digital region to the other digital region through the analog region.

If we now consider input signal voltages less than the threshold voltage, V_{Th}, as logic 0 and greater than, say, $2V_{Th}$ as logic 1 with outputs of 0 V and 5 V as logic 0 and logic 1 respectively, we then have a truth table as follows:

V_{in}	Logic in	Logic out	V_{out}
$< V_{Th}$	0	1	+5 V
$> 2V_{Th}$	1	0	0 V

In digital electronics, it is the central two columns with logic values of 0 and 1 that we will always be interested in but we we should never forget that these logic values are represented by voltages as indicated in the outer columns and that occasionally voltage levels can go outside these specified ranges leading to indeterminate or incorrect logic values. In particular, the transition between logic 0 and logic 1 is associated with a transition through the analog voltage region where the logic level is not defined so transitions in electronic circuits are often sources of problems.

The simple inverter shown in Figure 3.4 works well but has one major disadvantage. When a +5 V is present at the input the FET is ON and current flows through the 10 kΩ drain resistor. This current is not significant for a one inverter logic gate but if there are 100,000 gates in the integrated circuit the total current can be large and the heating effect can cause problems.

The solution is to use CMOS (Complementary MOS) where complementary p channel and n channel FETs are used. The two types of FETs can be fabricated together on a wafer by forming an n type diffused region within which a p channel MOSFET is fabricated as a mirror of the n channel MOSFET. The structure of the device as it is fabricated is shown in Figure 3.6. Note that this is a simplified structure of the device pair since there are a number of other buried diffused layers which are used to isolate the FETs from each other.

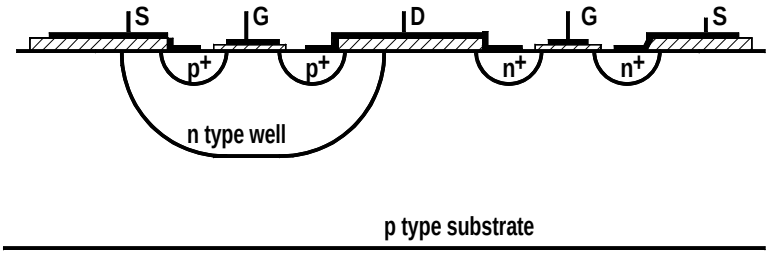

Figure 3.6: CMOS fabrication on a wafer.

The fabricated device shown in Figure 3.6 is used to form the electronic circuit shown in Figure 3.7. The crucial points to note in this figure are that the lower FET is an n channel FET and the upper FET is a p channel FET and that the two gates are connected together and that the two drains are connected together.

With a 0 V input present at the gates, the lower n channel FET is OFF but the upper p channel FET has a 5 V gate to source voltage which is greater that the V_{Th} for the FET and is therefore ON. This means that the output is connected to the +5 V through the conducting upper FET.

With a +5 V input present at the gate the lower n channel FET has a gate to source voltage greater than the V_{Th} and is ON. The upper p channel FET now has a 0 V gate to source voltage and is therefore OFF. The output is connected to 0 V through the conducting lower n channel FET.

The truth table is therefore the same as before and again gives inverter action. The difference in this configuration which makes it invaluable is that there is no quiescent current through both FETs. One or the other is

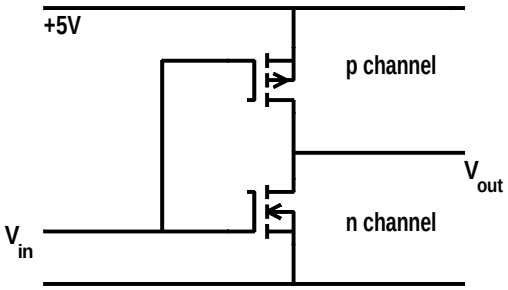

Figure 3.7: CMOS inverter.

always OFF (except possibly momentarily during the change over) so there is no significant current consumption in the circuit and therefore the power requirements are low and also the heat dissipated is low. Essentially each FET acts as the drain resistance for the other FET and the value of the effective drain resistance is very large (the source to drain resistance of an OFF FET) so there is little current though the circuit.

As a result, these devices are suitable for use in battery powered devices such as watches, calculators and portable computers where there are limitations on the power supplies and it also makes the devices suitable for more complex microcomputer systems employing many FETs which can be mains powered but which do not require cooling fans or heat exchangers to dissipate waste heat.

A logic inverter is a useful device but it is restricted in the complexity of the computation that it can carry out. The more useful configurations are the NOR and the NAND gates which we will now examine.

The CMOS structure for a two input NOR gate is shown in Figure 3.8 (a). In this circuit two n channel FETs are connected in parallel at the bottom of the circuit and there are two p channel FETs connected in series at the top. Each of the inputs, A and B, is connected to one of each of the n and p channel FETs. Also it should be apparent from an inspection of the circuit that the circuit is symmetrical with respect to the A and B inputs, that is the labels for the inputs A and B can be swapped without any change occurring in the circuit configuration.

In Figure 3.8 (b) a simple switch emulation of the NOR gate circuit is shown. The convention for the switches is that if A is open then $\overline{A}$ is closed and if A is closed then $\overline{A}$ is open.

It can be easily seen that the output of the switch circuit will be 0 V when one or both of the lower switches are closed and that the output can only be +5 V when both of the upper switches are closed and both of the lower

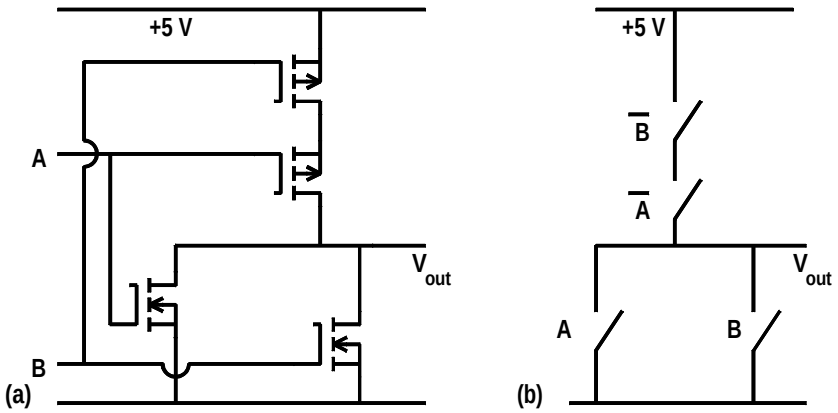

Figure 3.8: CMOS NOR gate and its switch equivalent.

switches are open. This then gives a truth table:

A	B	A	B	Logic out	V_{out}
Open	Open	0	0	1	5 V
Open	Closed	0	1	0	0 V
Closed	Open	1	0	0	0 V
Closed	Closed	1	1	0	0 V

If we consider the voltage signals A and B at the input to the CMOS NOR gate in Figure 3.8 (a) then application of +5 V to either input results in the corresponding lower n channel FET being ON and conducting and therefore giving an output voltage of 0 V. The corresponding upper p channel FET is OFF, disconnecting the power supply voltage from the output. Only when both lower FETs are OFF and both upper FETs are ON will the output be at +5 V or logic 1. The truth table for the FET circuit is then:

A	B	A	B	Logic out	V_{out}
0 V	0 V	0	0	1	5 V
0 V	+5 V	0	1	0	0 V
+5 V	0 V	1	0	0	0 V
+5 V	+5 V	1	1	0	0 V

Again in this table the central columns show the logic truth table and the outer columns show the physical voltages present at the inputs and the outputs.

The configuration for a CMOS NAND gate is shown in Figure 3.9 (a) with the equivalent switch emulation shown in Figure 3.9 (b).

In the switch emulation, if either of the upper switches is closed then the output is connected to the +5 V. Only if both lower switches are closed is

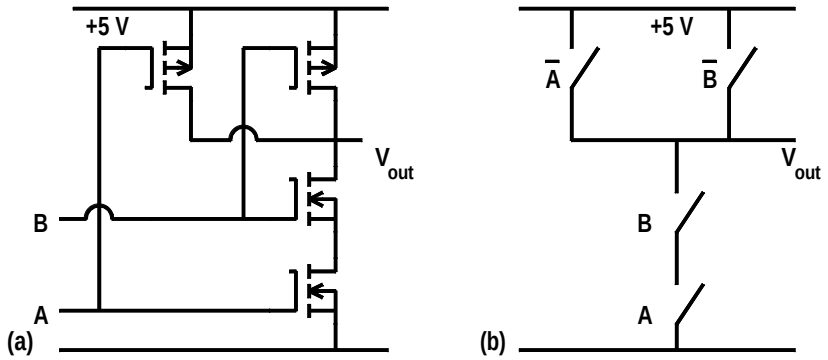

Figure 3.9: CMOS NAND gate and switch emulation.

the output connected to ground. This leads to the truth table for the switch circuit:

A	B	A	B	Logic out	V_{out}
Open	Open	0	0	1	5 V
Open	Closed	0	1	1	5 V
Closed	Open	1	0	1	5 V
Closed	Closed	1	1	0	0 V

Now consider the FET circuit in Figure 3.9 (a). Only when both of the inputs A and B are at +5 V will the two lower FETs be conducting and the two upper FETs be non-conducting so as to give a logic 0 at the output. The truth table is then:

A	B	A	B	Logic out	V_{out}
0 V	0 V	0	0	1	5 V
0 V	+5 V	0	1	1	5 V
+5 V	0 V	1	0	1	5 V
+5 V	+5 V	1	1	0	0 V

In the practical implementation of the CMOS logic gate circuit in the 4000 series family of devices, output buffering is employed which takes the logic output from circuits such as Figures 3.8 (a) and 3.9 (a) and adds in extra driver stages at the output. These are shown in Figure 3.10 for the NOR gate and in Figure 3.11 for the NAND gate..

The function of the output stages is to standardize delays within the circuit and to standardize the output drivers. The other advantages of buffering is that there is increased noise immunity because the increased voltage gain

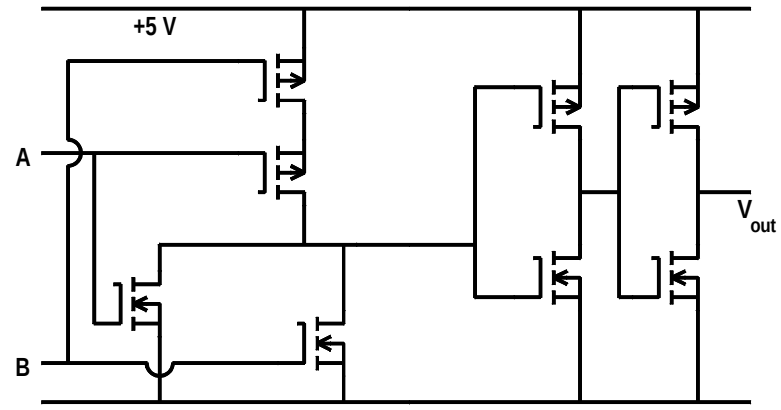

Figure 3.10: Buffered output NOR gate.

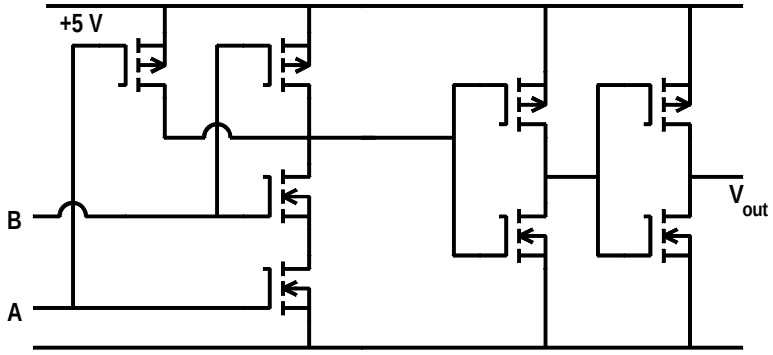

Figure 3.11: Buffered output NAND gate.

gives sharper transfer characteristics and narrows the analog region shown in Figure 3.5. The lower output impedance allows the buffered CMOS to drive the stray capacitance of the circuit board more easily and avoids RC smoothing of the signal line.

In addition to the main 4000 series CMOS logic gate family there are some subsets such as the HE4000 which have the output buffering features just discussed.