Unit 1 Electronic characteristics of ttl gates

- In transistor-transistor logic
  - a nominal 0 V represents a logic 0
  - a nominal +5 V represents a logic 1.
- Transistor-transistor logic gates operate as current sinking devices.

Digital electronics is based on the representation of signals in logic systems by the (two) binary logic symbols 0 and 1. These logic symbols are represented by electronic signal levels and before discussing logic systems it is appropriate that we first discuss the electronic circuits which are used to represent and to process logic signals. Unless the underlying electronic circuit behavior is understood, it is all too easy to construct a circuit which is logically correct but which fails to operate because of some electronic constraint which has been ignored.

The logic signals of 0 and 1 are usually represented by voltage levels having typical nominal values of 0 V and +5 V. So if we look at Figure 1.1 (a), we see that when the switch is closed, the voltage at the output is 0 V and that when the switch is open the voltage level is +5 V assuming that no current is drawn at the output.

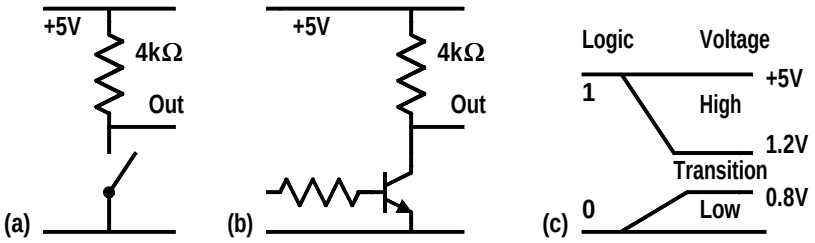

Figure 1.1: Voltage and logic levels in an inverter (NOT) gate.

This is, however, an idealized representation since we do not use mechanical switches but instead we use transistors to control the signals as is shown in Figure 1.1 (b). When the transistor is biased into conduction, there is a small V_{CE} between the emitter and the collector of the transistor. The

output voltage is then about 0.7 V and not the 0 V as was the case with the switch in (a). Similarly, when the transistor is biased off, there is still some small current in the transistor so there is a small voltage drop across the collector resistor and the output voltage is slightly less than the +5 V supply voltage.

Therefore it is necessary to replace the logical 0 and 1 not by specific voltages but by voltages which lie within certain permissible ranges. In TTL (Transistor Transistor Logic) a logic 0 is represented by a voltage between 0 V and +0.8 V and a logic 1 is represented by a voltage between +1.2 V and +5 V with a transition region between 0.8 V and 1.2 V through which the device switches very rapidly. This is shown is Figure 1.1 (c). It is at this early stage that digital electronics parts company with analog electronics. In analog electronics the operation of the circuits is usually constrained to this transition zone where there is a proportional relationship between the input voltage signal and the output voltage signal. In digital electronics the aim of the designer is to cause the circuit to spend the minimum of time in this transition zone so that switching between 0 and 1 signals is as rapid as possible. There is no logic signal for $\frac{1}{2}$ so any signal in the transition zone is an invalid signal. Note that the two voltages which bound the transition zone are quoted for TTL logic and may be different for other families of logic devices which use different power supply voltages.

In the circuits in Figure 1.1, the voltage levels are achieved by using either a switch or a transistor which can pass current and pull the voltage at the output down. This is called current sinking logic and is the usual configuration used in digital electronics. The principal advantages of the current sinking configuration are that it gives faster operation and facilitates the inter connection of circuits.

The circuit shown in Figure 1.1 (b) functions as an inverter, that is, a logic 1 or +5 V input gives a logic 0 or a nominal 0 V output and a 0 V input gives a logic 1 or +5 V output. If we call the input A and the output Q then truth table for such an inverter is shown below:

A	Q
0	1
1	0

However, this is not a very useful circuit since the input is not fully electronically compatible with the current sinking type of output and also a logic inverter, by itself, is not a computationally useful type of circuit.

The NAND gate circuit shown in Figure 1.2 is the basic circuit which is used in integrated circuit form throughout the TTL logic family (74XX

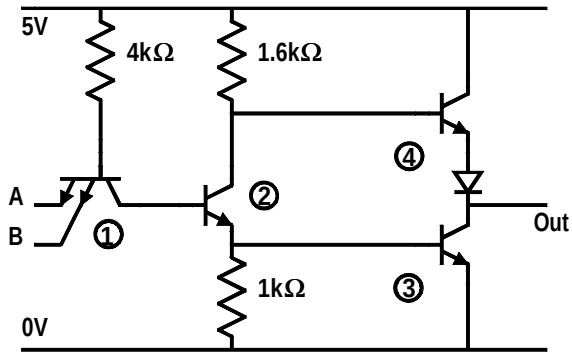

Figure 1.2: NAND (Negated output AND) gate circuit.

series devices) and displays the electronic features and properties which are characteristic of this logic family so it is important to fully understand the operation of the circuit.

The input signals are applied to A and B which constitute a dual emitter. It is important to realize that the two inputs, A and B, are not connected together but are two separate emitter regions within input transistor number 1. The basic constructional configuration of this input transistor is shown in Figure 1.3.

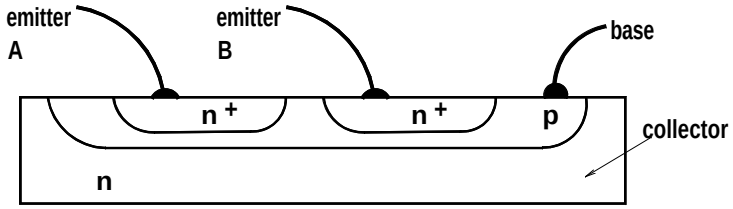

Figure 1.3: Double emitter construction of input transistor of a NAND gate.

There are two highly doped, n^+, emitter regions and the flow of current from either of these regions through the emitter-base junction to the collector in controlled by the emitter-base forward bias.

If the input emitters are at $+5\,\mathrm{V}$ or are left unconnected, then the emitter-base junction is reverse biased and the effective circuit for transistors 1 and 2 is that shown in Figure 1.4 (a) which leaves the base-collector effective diode acting as a forward biased diode giving current to the base of transistor 2 which is therefore conducting.

If either or both of the input emitters are grounded and are at $0\,\mathrm{V}$ then the effective circuit is that in Figure 1.4 (b) where the $4\mathrm{k}\Omega$ base bias resistor gives a forward bias on the base of transistor 1 and therefore gives a collector

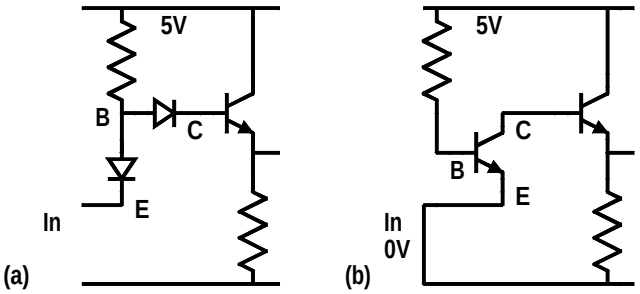

Figure 1.4: Input circuit for (a) 5V or unconnected input and (b) for 0V or grounded input.

current which effectively pulls down the voltage on the base of transistor 2 bringing it out of conduction.

Grounding one or both of the emitters of transistor 1 puts the transistor into conducting mode so that the collector voltage drops. It is only when both of the inputs to transistor 1 are unconnected or at +5 V that the base-collector diode becomes forward biased allowing a current to the base of transistor 2. The dual emitter input transistor therefore performs an AND function.

We can now trace the operation of the other two transistors of Figure 1.2. When transistor 2 is conducting, transistor 3 has base current and pulls the output voltage down towards 0 V. When transistor 2 is not conducting, there is no base current for transistor 3 but there is base current for transistor 4 which flows through the 1.6 kΩ resistor and transistor 4 is ON and the output voltage is high. The function of diode between transistors 3 and 4 is to prevent the emitter to collector voltage of transistor 2 from turning on both of transistors 3 and 4 simultaneously and shorting out the power supply.

The table below shows the states of the circuit transistors of the NAND gate circuit for four possible valid input to the truth table. It should also be noted that an unconnected input (N.C.= no connection) defaults to a +5 V input. It is not recommended that this be allowed to happen as any unconnected input can act as an antenna and may pick up signals at random from other parts of the circuit and give an indeterminate and unpredictable output as a result.

A	B	1	2	3	4	OUT
0 V	0 V	ON	OFF	OFF	ON	+5 V
5 V	0 V	ON	OFF	OFF	ON	+5 V
0 V	5 V	ON	OFF	OFF	ON	+5 V
5 V	5 V	B-C Forward biased	ON	ON	OFF	0 V
N.C.	N.C.	B-C Forward biased	ON	ON	OFF	0 V

We have seen that the input to this NAND gate requires either a +5 V or unconnected input for a logic 1 input and a grounded or current sinking input for a logic 0 input. We have seen that the output from the NAND gate is either a +5 V signal or a transistor which sinks the output to ground. The output configuration is therefore compatible with any other logic gates which may be connected to the output since we have current sinking logic for both output and inputs. This is the situation which is illustrated in Figure 1.5 where the TTL circuit, of whatever logic function, is contained within the outline box.

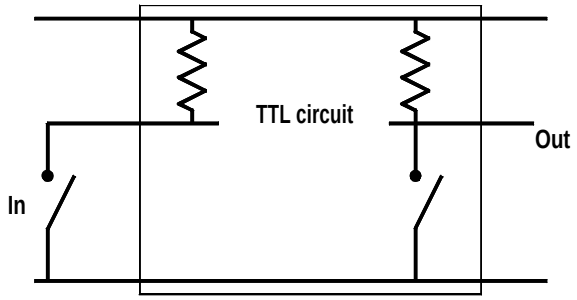

Figure 1.5: Effective current sinking input and output.

1.1 Problems

1.1 Would two separate NPN transistors give the same function as transistor 1 in Figure 1.2? Justify your answer.

1.2 A light emitting diode which illuminates when the current through the led is 10 mA is to be connected to the output of a NAND gate. A resistor is placed in series with the led to limit the current to the permitted value.

Should the led and resistor be connected (a) between the NAND gate output and ground OR (b) between the NAND gate output and the +5 V supply? Sketch the two circuit configurations. Justify your answer by reference to the circuit in Figure 1.5.

1.3 What does the "N" in "NAND" and "NOR" signify?

1.4 Draw up truth tables for AND, NAND, OR and NOR gates.

1.5 How would you connect a two input NAND gate so as to form a NOT gate (an inverter)?

1.6 How would you connect two NAND gates so as to form an AND gate?

1.7 Explain the operation of the NOR gate shown in Figure 1.6.

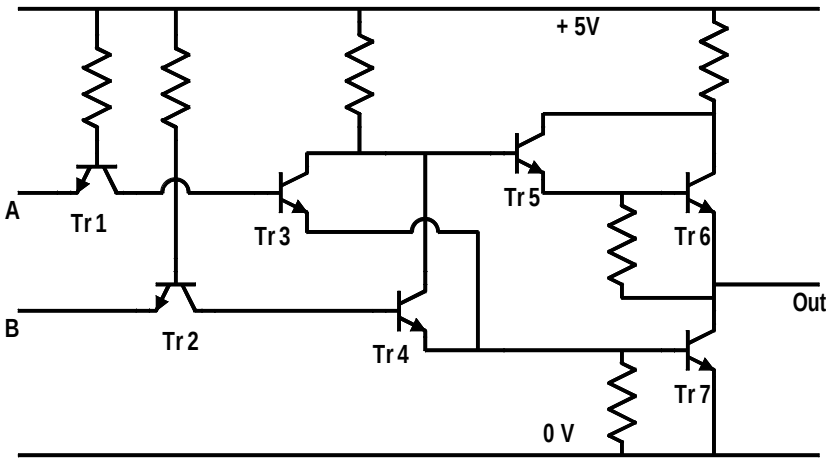

Figure 1.6: NOR gate