Unit 27 Asynchronous Sequential Circuits

- If there is feedback in a circuit, then the circuit will have a memory and can not be expressed as a Boolean Sum of Products.

- Asynchronous sequential circuits do not wait for a clock pulse before changing the output.

- Asynchronous sequential circuits change the output one propagation delay time after the primary input changes.

- The system will only be in a stable state if the next state and the present state are the same.

- Stable states are those states for which the q values in the **Excitation map** are the same in each column.

- The **flow table** shows the sequence of stable states.

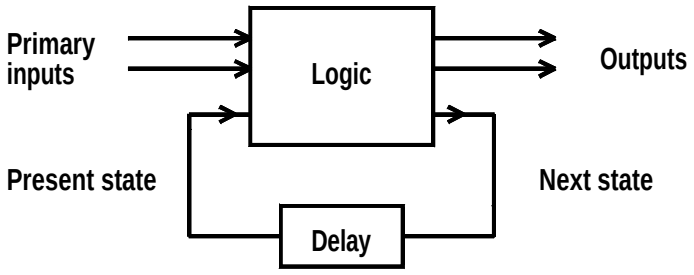
- The flow table allows the preparation of the **State diagram**.

Unit 27 Asynchronous Sequential Circuits

Course Structure

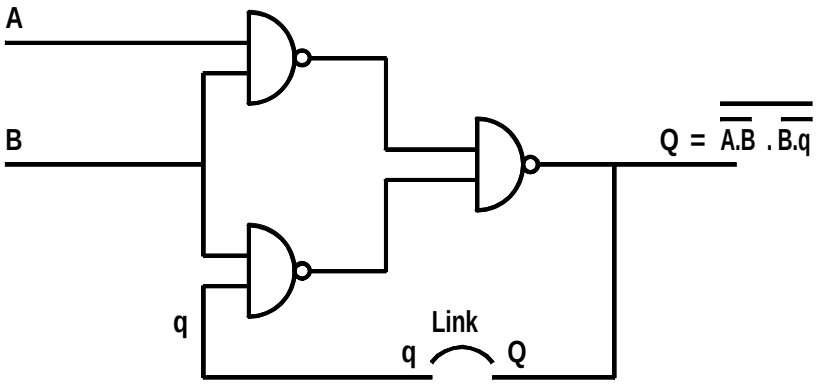
- Combinational Logic circuits
- Sequential circuits
- Asynchronous Sequential Circuits

Unit 27 Asynchronous Sequential Circuits



The system will be in a stable state if the next state and the present state are the same.

Unit 27 Asynchronous Sequential Circuits



Break Link

Compare q and resulting Q

$$Q = \overline{\overline{A.B}.\overline{B.q}} = A.B + B.q$$

Prepare **Excitation Map**
Primary inputs at top of column

	AB			
	00	01	11	10
$q = 0$	0	0	1	0
$q = 1$	0	1	1	0

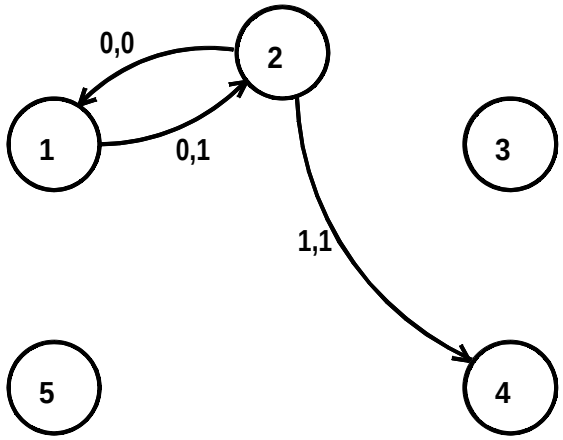
Stable if $q = Q$

	AB			
	00	01	11	10
$q = 0$	(1)	(2)	4	(5)
$q = 1$	1	(3)	(4)	5

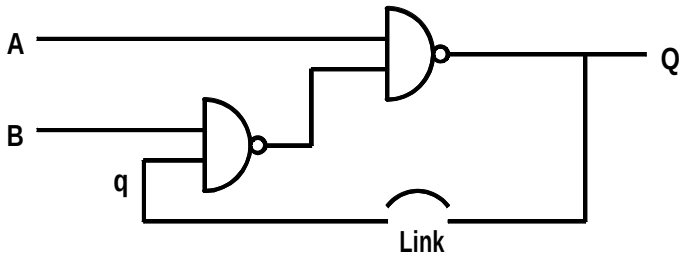
Flow Table.

	AB			
	00	01	11	10
$q = 0$	(1)	(2)	4	(5)
$q = 1$	1	(3)	(4)	5

Flow Table.



Partial state diagram



RS flip flop diagram.

$$Q = \overline{\overline{B.q}.A} = \overline{A} + \overline{\overline{B.q}} = \overline{A} + B.q$$

	AB			
	00	01	11	10
$q = 0$	1	1	0	0
$q = 1$	1	1	1	0

Excitation Map for Q

	AB			
	00	01	11	10
$q = 0$	1	1	0	0
$q = 1$	1	1	1	0

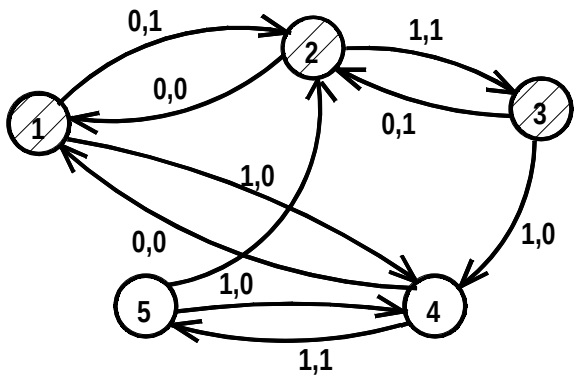
Excitation Map for Q

	AB			
	00	01	11	10
$q = 0$	1	2	(5)	(4)
$q = 1$	(1)	(2)	(3)	4

Flow Table.

	AB			
	00	01	11	10
$q = 0$	1	2	(5)	(4)
$q = 1$	(1)	(2)	(3)	4

Flow Table.



State Diagram.