- Sequential circuits contain memory devices and have a state memory.

- Synchronous sequential circuits move from one memory state to another under the control of a set of inputs and at a time determined by an external clock.

- Sequential circuits are modeled by **Mealy** or by **Moore** machine models.

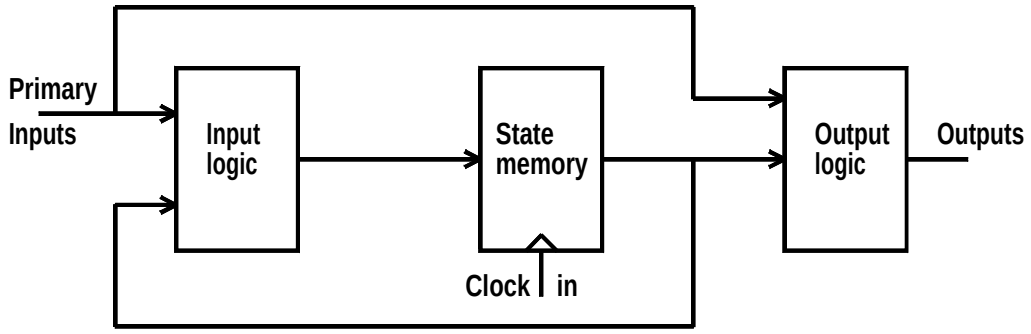
- The state machines are described either by **state tables** or by **state diagrams**.

- Procedures exist for converting between Mealy and Moore machine models.

Sequential circuit determined by:

- Inputs to the circuit.
- Present circuit state

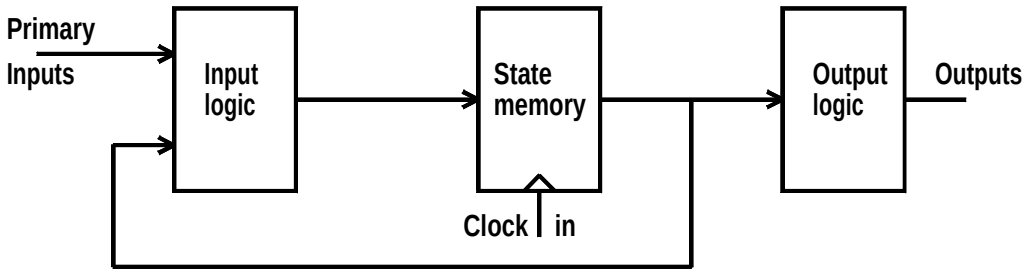
Examples: A counter, A coffee machine.



Mealy machine model.
Present output state determined by

- Present external inputs (Primary inputs)
- State memory after previous clock cycle

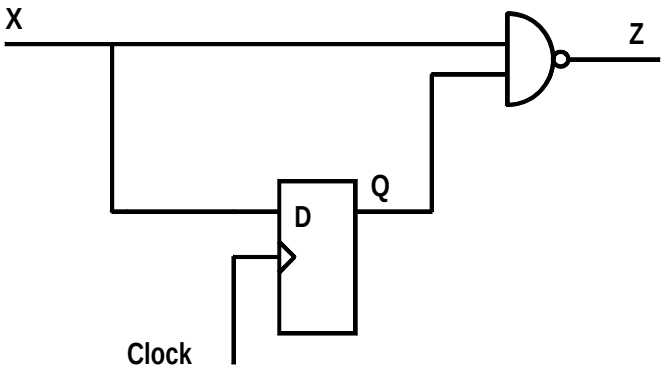
Note that Primary Input can propagate to output without waiting for a clock pulse.



Moore machine model is a special case of Mealy machine.

Output determined by present state memory which is set at last clock pulse.

The Primary Input can change without changing the output.



Simple sequential machine.
D type flip flop forms the memory.

Present state	Input	
Q	X = 0	X = 1
0	0,1	1,1
1	0,1	1,0

Mealey Model **State table** (Next State, Output).

Mealy Model State Table

Present state Q	Input X = 0	Input X = 1
0	0,1	1,1
1	0,1	1,0

For input X = 0
Next state and output, (Q,Z), must be (0,1)
because a 0 is read into the flip flop
and NAND gate gives a Z = 1 output

For input X = 1,
Next state, (Q,Z), is (1,0) for present state
Q = 0
and (1,1) for present state Q = 1.

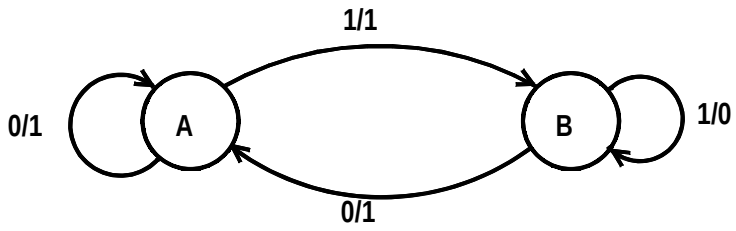
Mealy Model

Present state Q	Input X = 0	Input X = 1
A	A,1	B,1
B	A,1	B,0

General rules for State Table labels.
Label rows with letters
Table entries are (Q,Z) = (Next state, Output)

Present state	Input		
Q	X = 0	X = 1	Output
A	A	C	1
B	A	B	0
C	A	B	1

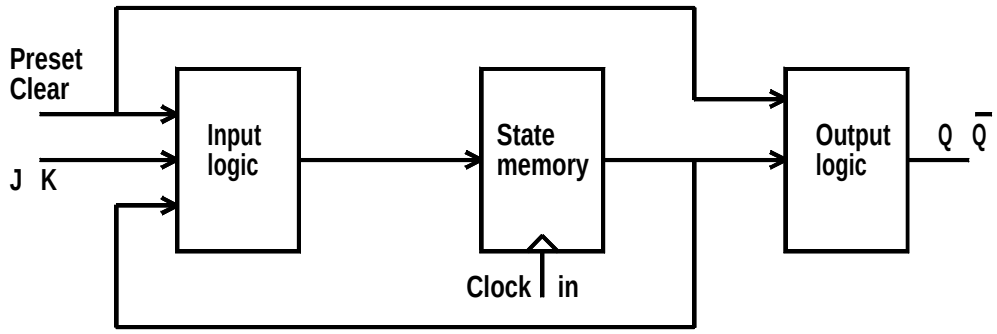
A Moore model state table
(present state) is the state table entry.
Inputs can bypass memory to reach output.
Where the states are now defined by
Q = (Memory state,Output),
A = 0,1, B = 1,0 and C = 1,1.



State diagram. for the Mealy model
Distinct memory states represented by labeled circles
Transitions are represented by edges connecting the states.
Numbers beside the edges are the input and output in form X/Z.
This can give either output 0 or 1 depending on the last edge which was traversed.

Inputs					Outputs	
Preset	Clear	Clock	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	$\downarrow$	L	L	Q_0	$\overline{Q_0}$
H	H	$\downarrow$	H	L	H	L
H	H	$\downarrow$	L	H	L	H
H	H	$\downarrow$	H	H	$\overline{Q_0}$	Q_0
H	H	H	X	X	Q_0	$\overline{Q_0}$

Function table for 74LS76A JK flip flop



Mealy machine model for 74LS76 JK flip flop.

Conversion between Moore and Mealy models

- A Moore model has a unique set of outputs for each internal memory state
- The Mealy model does not have a unique set of outputs for each internal memory state.
- The Mealy model can change at times other than at the clock edge because the inputs can bypass the memory.

Present state	Input X = 0	X = 1
A	D,0	E,0
B	A,1	A,0
C	B,1	C,1
D	A,0	B,1
E	C,0	D,0

Mealy circuit state table: convert to Moore model

Identify all of the distinct sets of (Next state, Output) combinations
Generate a row in the Moore state table for each combination.

A,0	A,1	B,1	C,0	C,1	D,0	E,0
P	Q	R	S	T	U	V

A,0 P	A,1 Q	B,1 R	C,0 S	C,1 T	D,0 U	E,0 V

Present state	Input $X = 0$	Input $X = 1$	Output
A,0	D,0	E,0	0
A,1	D,0	E,0	1
B,1	A,1	A,0	1
C,0	B,1	C,1	0
C,1	B,1	C,1	1
D,0	A,0	B,1	0
E,0	C,0	D,0	0

Equivalent Moore circuit state table

Present state	Input X = 0	Input X = 1	Output
A,0	D,0	E,0	0
A,1	D,0	E,0	1
B,1	A,1	A,0	1
C,0	B,1	C,1	0
C,1	B,1	C,1	1
D,0	A,0	B,1	0
E,0	C,0	D,0	0

Equivalent Moore circuit state table

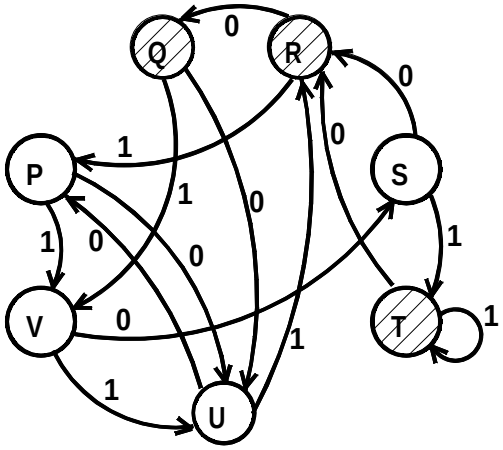
Which gives:

Present state	Input X = 0	Input X = 1	Output
P	U	V	0
Q	U	V	1
R	Q	P	1
S	R	T	0
T	R	T	1
U	P	R	0
V	S	U	0

Equivalent Moore circuit state table

Present state	Input X = 0	Input X = 1	Output
P	U	V	0
Q	U	V	1
R	Q	P	1
S	R	T	0
T	R	T	1
U	P	R	0
V	S	U	0

Equivalent Moore circuit state table



Complete state diagram (Moore model).

Moore to Mealy conversion

Combine the next state columns with the output columns

Generate a (Next state, output) pair Mealy state table.

Present state	Input $X = 0$	Input $X = 1$	Output
A	B	A	0
B	E	F	1
C	D	B	1
D	C	A	0
E	A	D	0
F	E	C	1

Moore circuit state table

Present state	Input X = 0	Input X = 1	Output
A	B	A	0
B	E	F	1
C	D	B	1
D	C	A	0
E	A	D	0
F	E	C	1

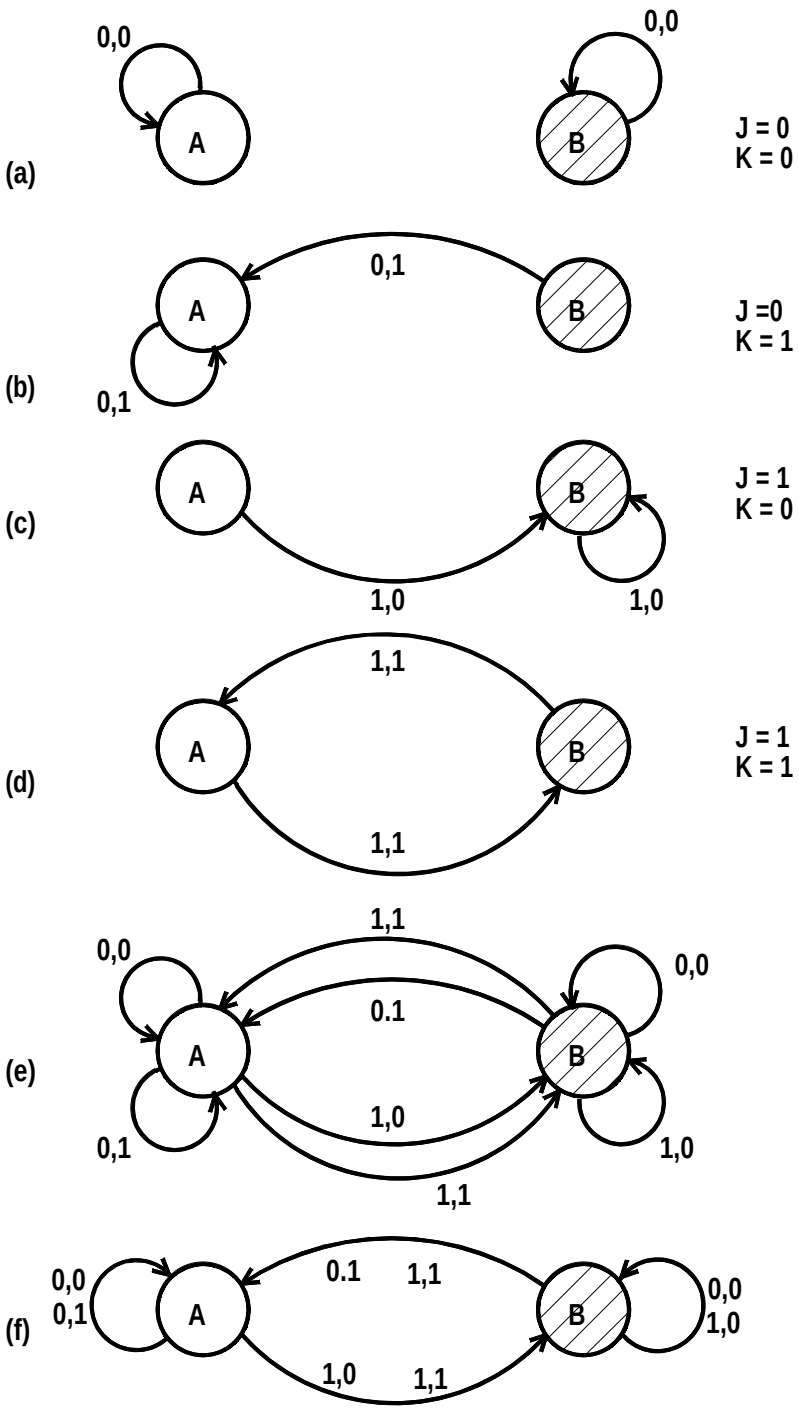
Moore circuit state table

Present state	Input X = 0	Input X = 1
A	B,1	A,0
B	E,0	F,1
C	D,0	B,1
D	C,1	A,0
E	A,0	D,0
F	E,0	C,1

Equivalent Mealy circuit state table

Construct the state diagram for a JK flip flop using a Moore model. Assume that the Preset and Clear are not used.

Unit 26 Sequential circuit models


(a)
0,0
A
0,0
B
J = 0
K = 0
(b)
0,1
A
B
0,1
J =0
K = 1
(c)
A
B
1,0
1,0
J = 1
K = 0
(d)
1,1
A
B
1,1
J = 1
K = 1
(e)
1,1
0,0
0,0
0.1
A
B
1,0
0,1
1,0
1,1
(f)
0,0
0,1
0.1
1,1
A
B
0,0
1,0
1,0
1,1