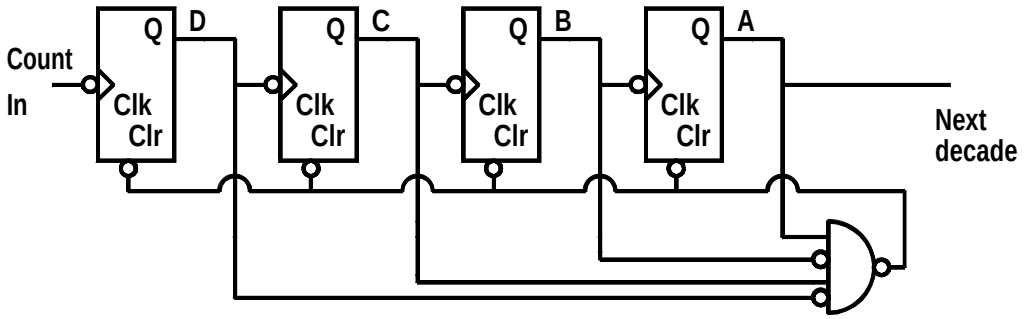
- Base 2 binary counters can be used to construct base m counters by a Clear instruction when the modulus is reached.

- A Down counter counts down from an initial binary number when the $\overline{Q}$ output of the binary counters is used for interstage transfer.

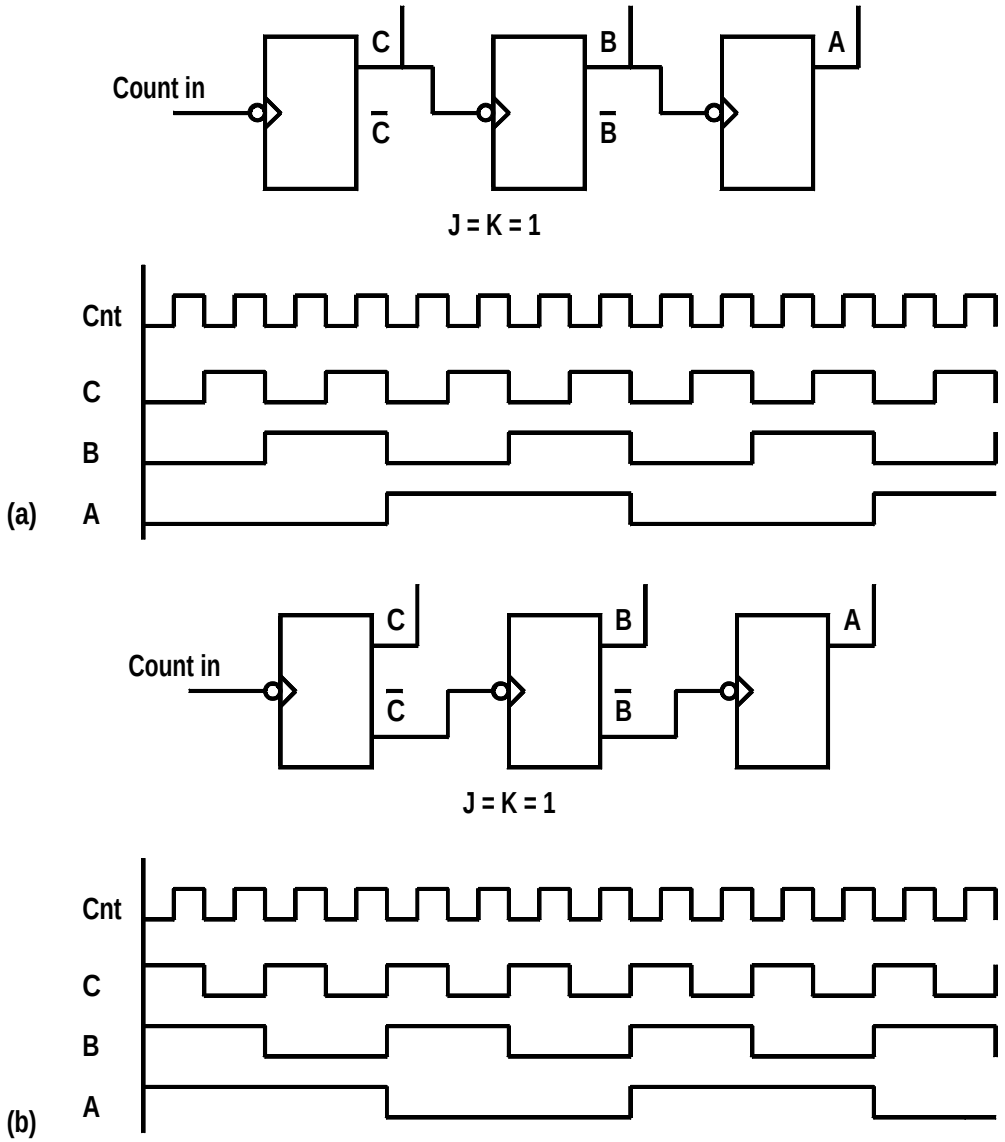
- The count ripples through asynchronous counters.

- All of the stages of a synchronous counter change state at the same time.

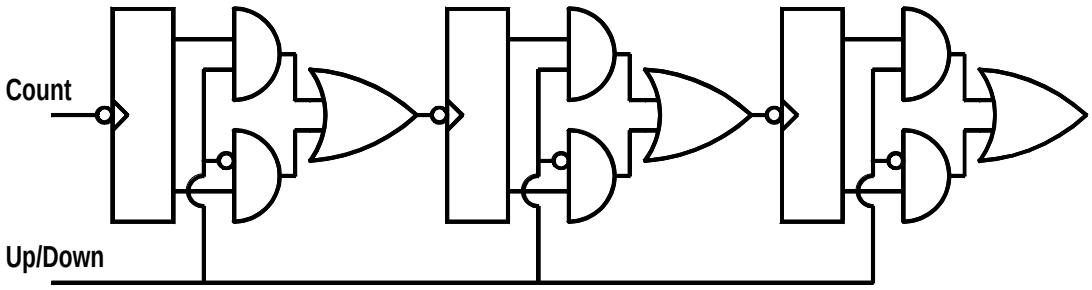


Modulo 10 Counter.

When the output $Z = 1001$ is reached next count gives the output $Z_{10} = 1010$ NAND gates generate a reset to zero

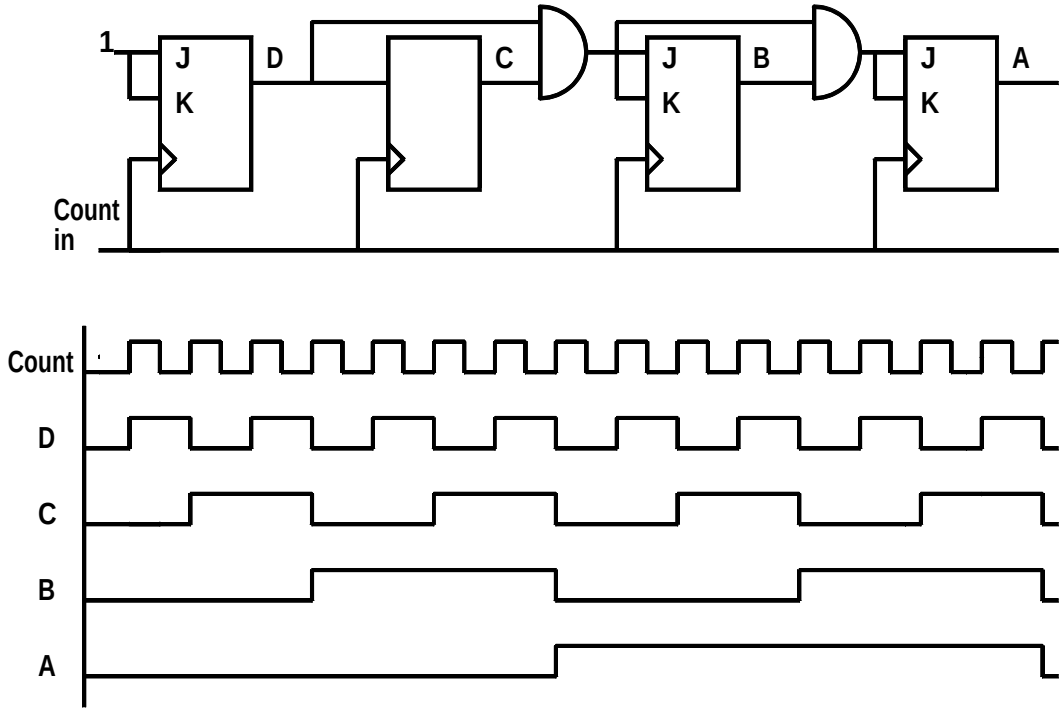


(a) 3 bit up counter. (b) 3 bit down counter.



Switchable 3 bit up/down counter.

The u/d input allows the direction of count to be switched as required.
The AND/OR gates select the signals applied to the clock inputs from either the Q or the $\overline{Q}$ outputs from the flip flops.



Synchronous counter and counting waveforms.

All of the outputs change state simultaneously

Avoids readout problems at the expense of increased circuit complexity.

Incoming count pulse fed to all binary counter stages simultaneously.