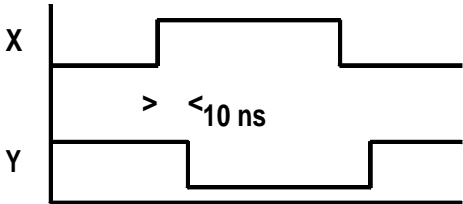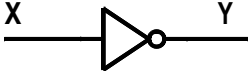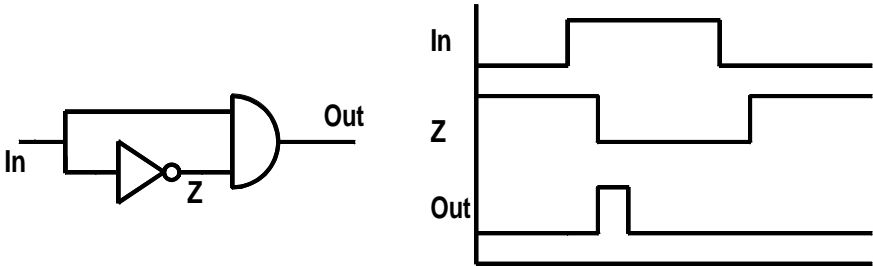- In a JK flip flop the indeterminate output state is replaced by a toggled output.

- The Master-Slave flip flop avoids racing by splitting the reading in operation and outputting function into two steps which occur on opposite edges of the clock pulse.

- When J = K = 1, a JK flip flop will operate as a single stage binary counter.

X ──▷o── Y

X

> <10 ns

Y

In

Out

In

Z

Z

Out

Positive Edge Gate generator
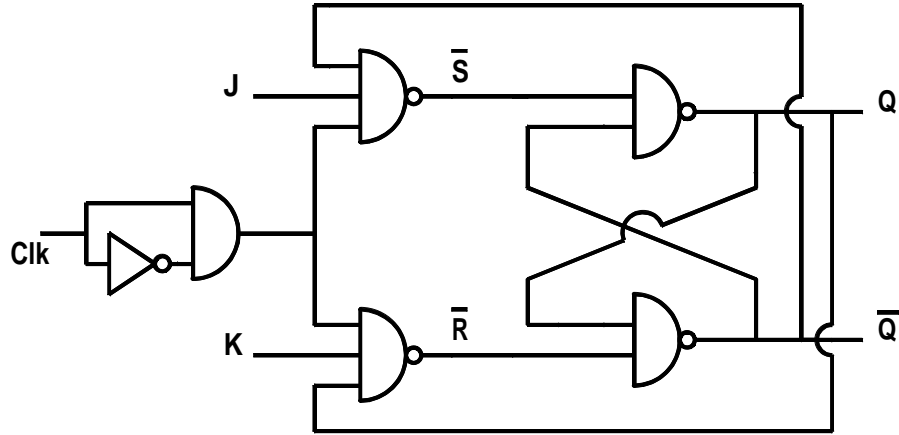
$\overline{R}$	$\overline{S}$	Q	$\overline{Q}$
1	1	Q_{Old}	$\overline{Q}_{Old}$
1	0	1	0
0	1	0	1
0	0	?	?

| Clk	J	K	Q_{Old}	$\overline{R}$	$\overline{S}$	Q_{New}	Comments
0	X	X	X	1	1	Q_{Old}	No change
↑	0	0	X	1	1	Q_{Old}	
↑	0	1	0	1	1	0	
↑	0	1	1	0	1	0	
↑	1	0	0	1	0	1	
↑	1	0	1	1	1	1	
↑	1	1	0	1	0	1	Toggles
↑	1	1	1	0	1	0	Toggles

Rules for the operation of the Positive Edge triggered JK flip-flop:

1. Nothing changes in the absence of a positive edge on clock input.

2. When a positive clock edge occurs:

   (a) If J = 0 and K = 0 then no change

   (b) If J = 1 and K = 0 then Q → 1

   (c) If J = 0 and K = 1 then Q → 0

   (d) If J = 1 and K = 1
       then Q toggles (1 → 0 or 0 → 1)

There is an ambiguity in JK truth table.
Edge trigger is not really an edge trigger.
It ia actually a short duration level trigger.
If input changes during this short time then
the output can toggle.
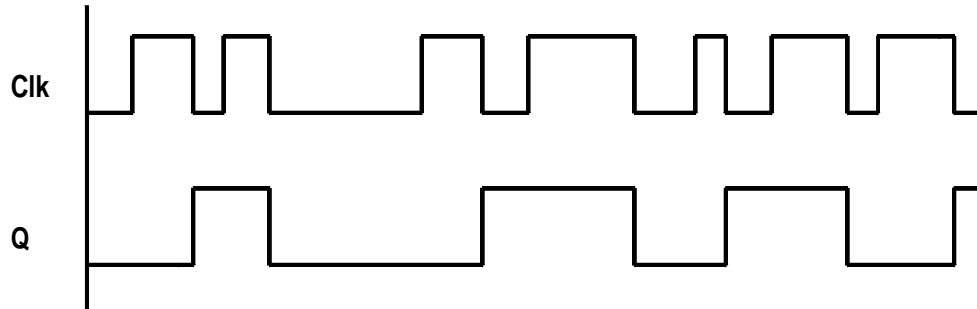This is called the **racing problem**
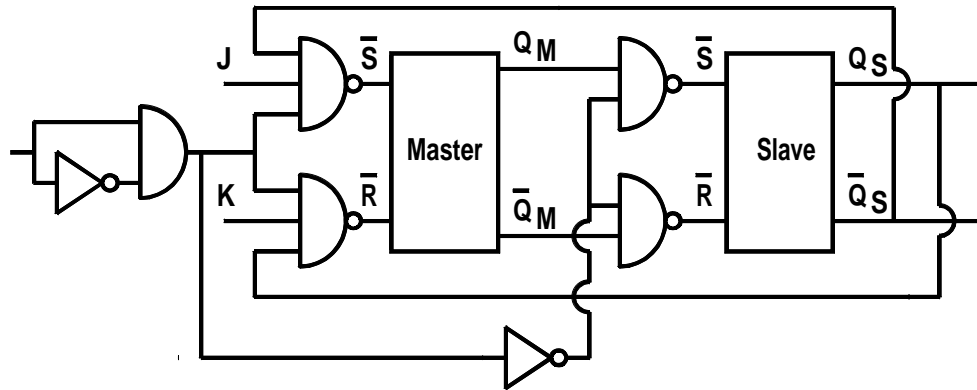
Master-Slave JK flip flop.

For $J = K = 1$ a clock edge gives a 1 at $\overline{R}$ input of master.

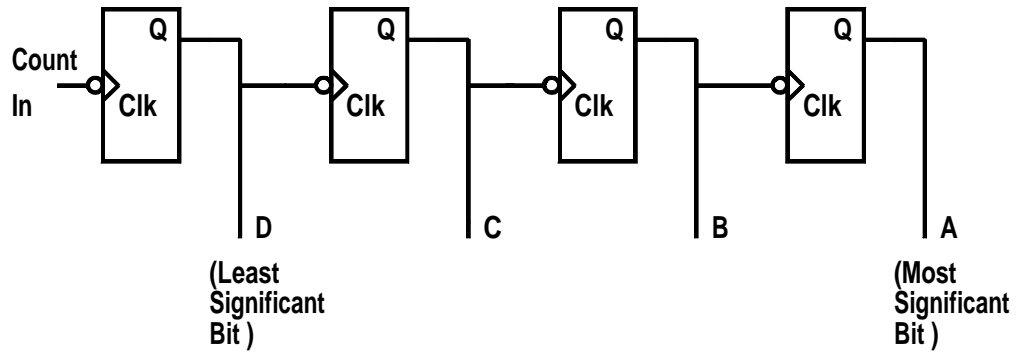The next negative clock edge transfers this to the slave.

The two step operation avoids the possibility of racing.
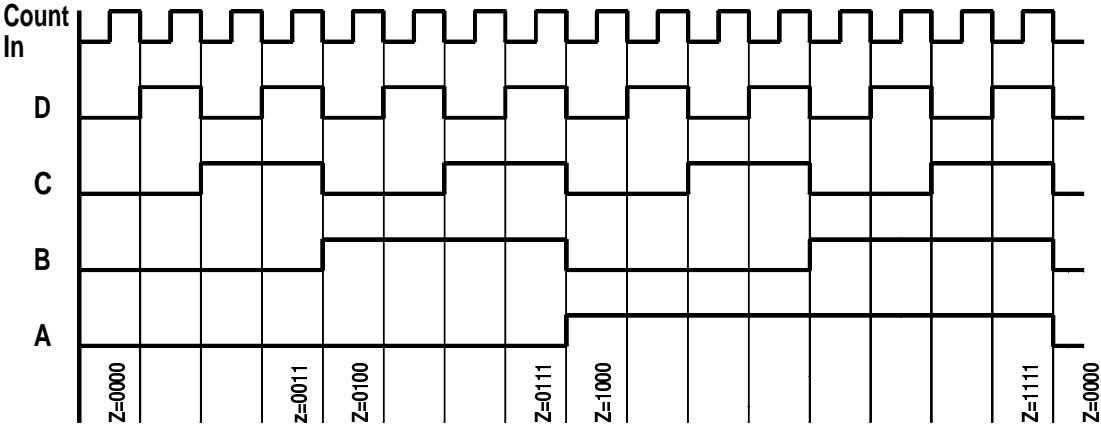

JK flip flops can be used for counting.

Use the toggling action when $J = K = 1$.

This makes a single stage binary counter.

Counter configuration. $J = K = 1$ (not shown).

Multistage binary counter

Waveform observed on a five channel oscilloscope for the four bit binary counter.