- Feedback circuits such as flip flops are analyzed by cutting the feedback loop and applying signals to the open circuit.

- A flip flop is stable in either of two states.

- A RS flip flop can be switched between stable states by application of a Reset or Set input.

- D type flip flops use an inverter at the input to prevent the occurrence of an indeterminate state.

- Gated flip flops can only make transitions when a gate or clock pulse is present or at the positive or negative going edge of a clock pulse.

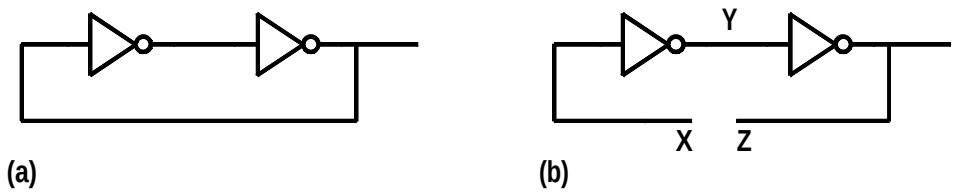
Unit 22 RS and D type Flip-Flops

Units 1 to 19 examined

- Time independent circuits—static circuits.
- Circuits in which the signals only propagate in the forward direction.

We now introduce

- Signal feedback.
- Time dependence

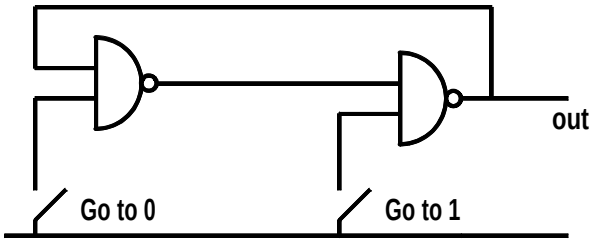


NOT gate feedback latch circuit.

Cut and apply an external signal at the point X. The input signals, X, intermediate signals, Y, and the resulting output or feedback signals, Z, are shown in the table.

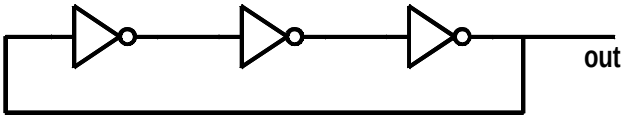
X	Y	Z
0	1	0
1	0	1

When the input and output signals match there will be no change to the circuit if a connection is made across the cut.
This is therefore a circuit which is stable in either state.



Use of NAND gates allows inputs to be applied to change the state of the latch.

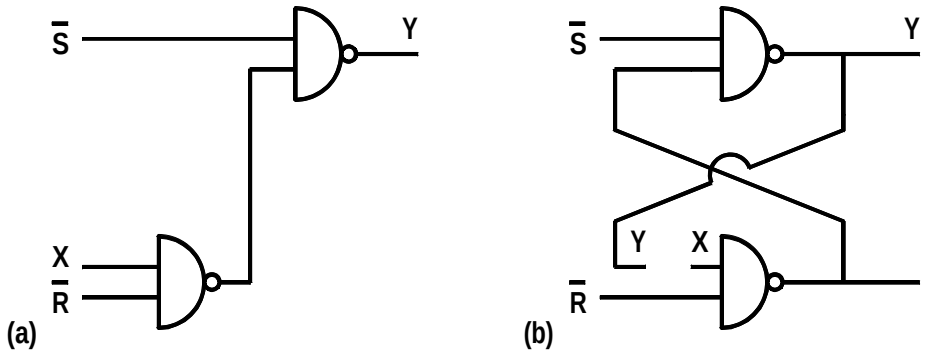
This latching circuit retains a memory of the state to which it was last driven.



Three inverter NOT gate feedback circuit..

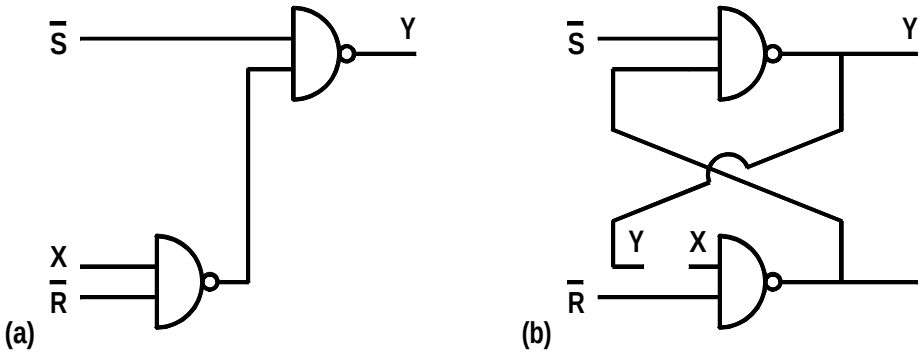
In	Out
0	1
1	0

The logic signals at each side of the cut are inconsistent so the circuit will not be stable. The circuit oscillates with a periodic time, T, which is six times the signal propagation delay in each of the inverter NOT gates.



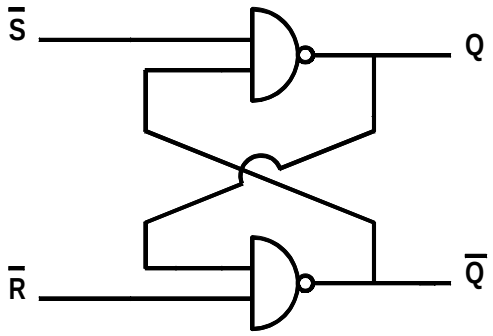
NAND gate version of RS flip flop.

Three inputs: $\overline{S}$ (set), $\overline{R}$ (reset) and X and a single output, Y.
Redraw to emphasize the symmetry of the circuit



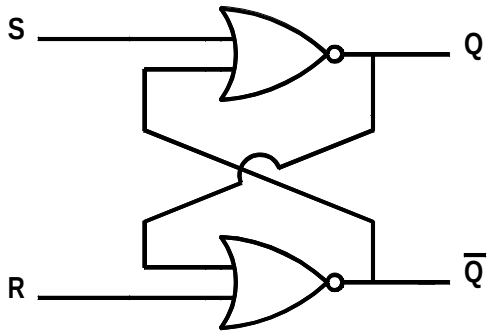
$$Y = \overline{\overline{X.\overline{R}.\overline{S}}} = \overline{\overline{X.\overline{R}}} + \overline{\overline{S}} = X.\overline{R} + \overline{\overline{S}}$$

$\overline{R}$	$\overline{S}$	X	Y	X = Y ?
0	0	0	1	Unstable
0	1	0	0	Stable
1	0	0	1	Unstable
1	1	0	0	Stable
0	0	1	1	Stable
0	1	1	0	Unstable
1	0	1	1	Stable
1	1	1	1	Stable



$\overline{R}$	$\overline{S}$	Q	$\overline{Q}$
1	1	Q	$\overline{Q}$
1	0	1	0
0	1	0	1
0	0	?	?

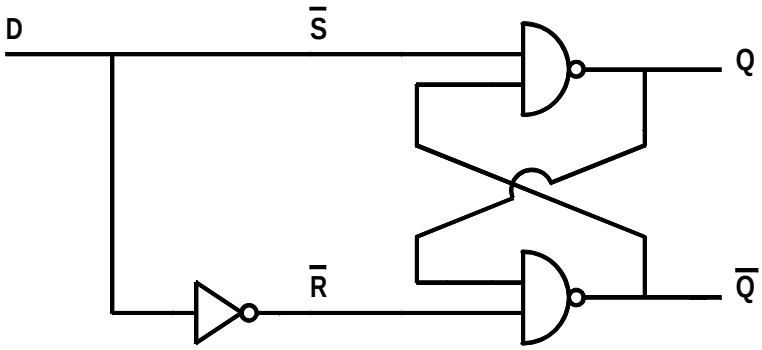
NAND gate version of RS flip flop and truth table. Active LOW.



R	S	Q	$\overline{Q}$
1	1	?	?
1	0	1	0
0	1	0	1
0	0	Q	$\overline{Q}$

NOR gate version of the RS flip flop. Active HIGH

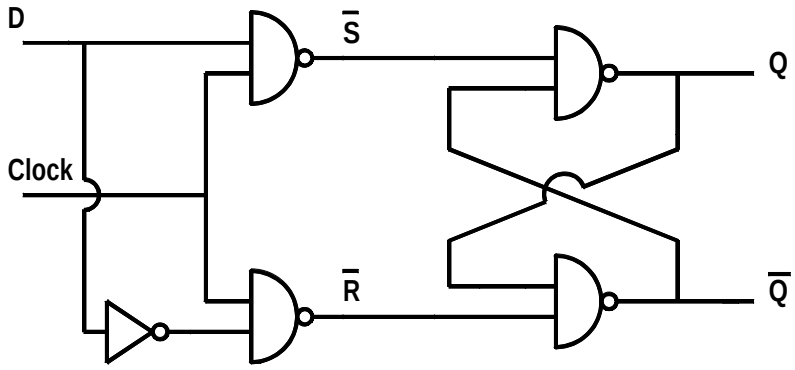
Truth table is slightly different
The indeterminate state now occurs for inputs of $R = 1$ and $S = 1$ and the latched state occurs for inputs of $R = 0$ and $S = 0$



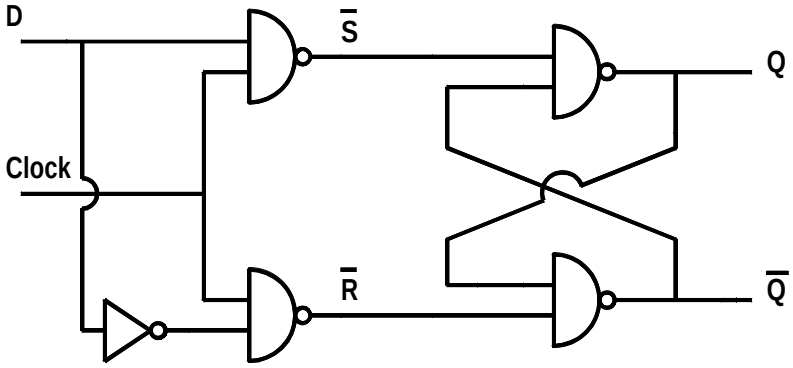
D type flip flop.

The indeterminate state can be prevented from occuring by including an inverter.

This new type of circuit is called a D type flip flop.

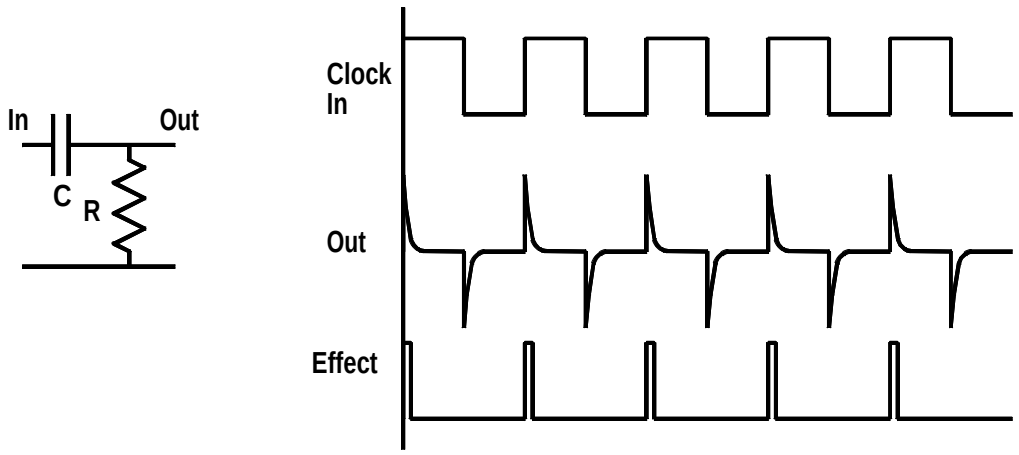


Gated D type flip flop.
Synchronization of different parts of a circuit
Use a square clock synchronization waveform
Require that all state transitions in the circuit only occur when the clock is in its logic 1 half cycle.



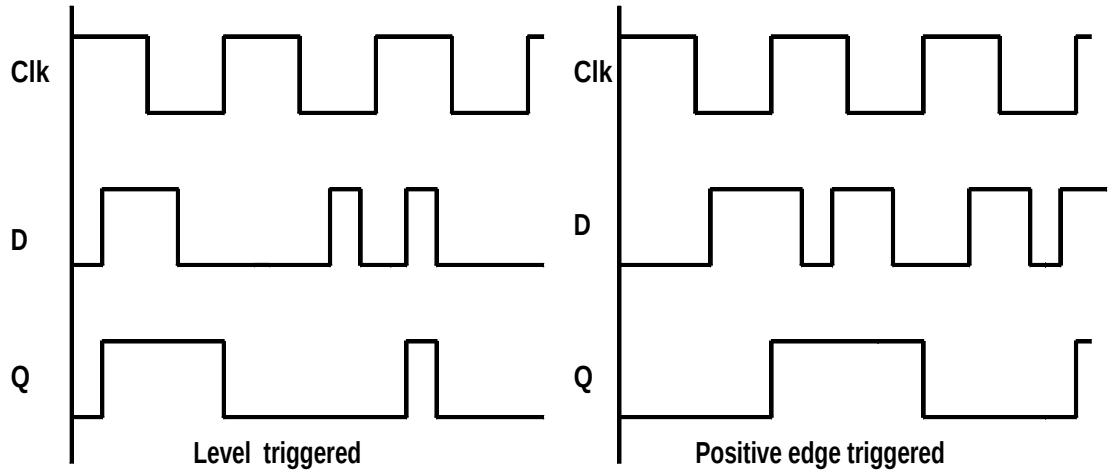
Clk	D	$\overline{S}$	$\overline{R}$	Q	$\overline{Q}$
0	X	1	1	Q	$\overline{Q}$
1	0	1	0	0	1
1	1	0	1	1	0

When an input is shown as an X then the logic state for that input is irrelevant.
Rule for gated D type flip flop is that the logic state of the D input is transferred to the Q output while the clock is at logic 1.



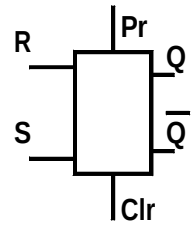
Differentiation of a square waveform.

The duration of the spikes will depend on the time constant, $T = RC$, for the CR filter. This gives an Edge triggered D type flip flop.

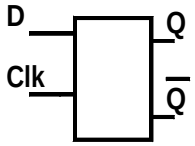


Timing waveforms for level and edge triggered D type flip flops.

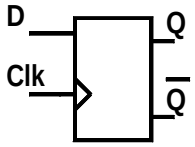
Unit 22 RS and D type Flip-Flops



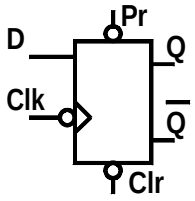
RS Flip Flop with Preset and Clear



D type Flip Flop with level triggered clock



D type Flip Flop with Positive edge triggered clock



D type Flip Flop with negative edge triggered clock

Typical circuit schematics for D type flip flop versions.

Inputs				Outputs		Comment
Pr	Clr	Clk	D	Q	$\overline{Q}$	
L	H	X	X	H	L	Preset
H	L	X	X	L	H	Cleared
L	L	X	X	H*	H*	Unstable
H	H	$\downarrow$	H	H	L	Transfer D$\rightarrow$Q
H	H	$\downarrow$	L	L	H	Transfer D$\rightarrow$Q
H	H	$\uparrow$	X	Q_o	$\overline{Q_o}$	No change
H	H	H	X	Q_o	$\overline{Q_o}$	No change
H	H	L	X	Q_o	$\overline{Q_o}$	No change

Typical data book specification for Negative Edge Triggered D type Flip-Flop.