- A PLD is a universal Sum of Products circuit in which input Product and output Sum combinations are selected by either fusing links or by activating memory transistor links within the integrated circuit.

- This customization gives an application specific integrated circuit (ASIC) at low cost.

- In bipolar technology devices the fuses are metal links which can be melted by application of a current.

- In CMOS devices the links are transistors which are open circuit when supplied by the manufacturer and can be closed during the programming.

- The CMOS devices are Electrically Erasable and can be reprogrammed.

- **JEDEC** stands for Joint Electronic Devices Engineering Council which sets standards in the industry.

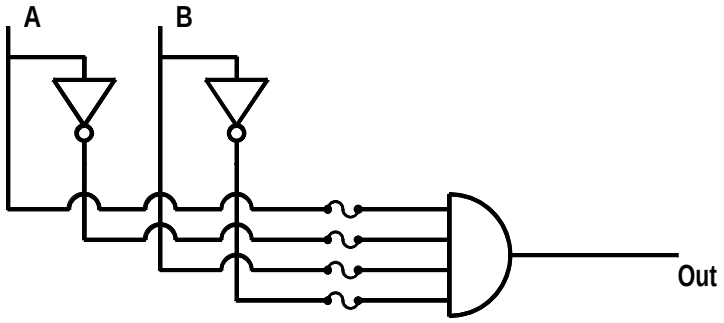
- **PROM**—Programmable Read Only Memory, AND inputs fixed, OR inputs programmable .

- **PAL**—Programmable Array Logic, AND inputs programmable, OR inputs fixed.

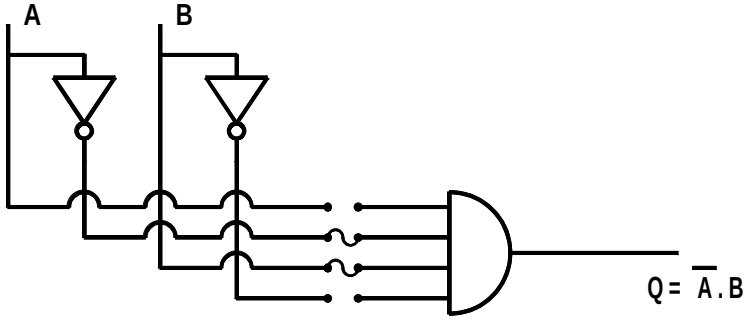
- **PLA**—Programmable Logic Arrays, both AND and OR gates programmable.

- **GAL**—Gate Array Logic.

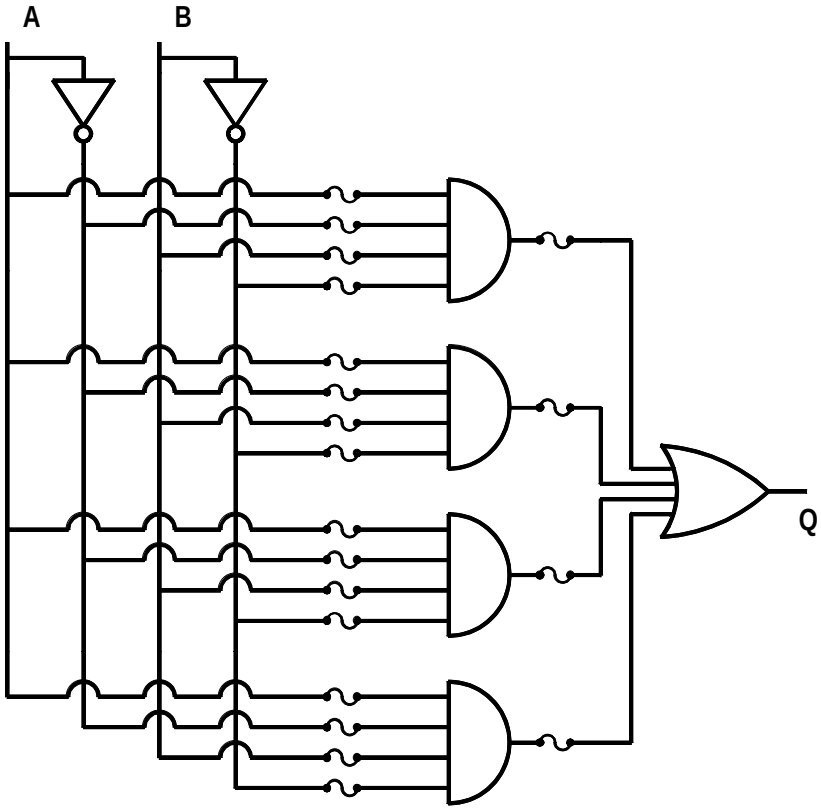
- **FPLA**—Field Programmable Logic Array, the fuses can be blown by the user



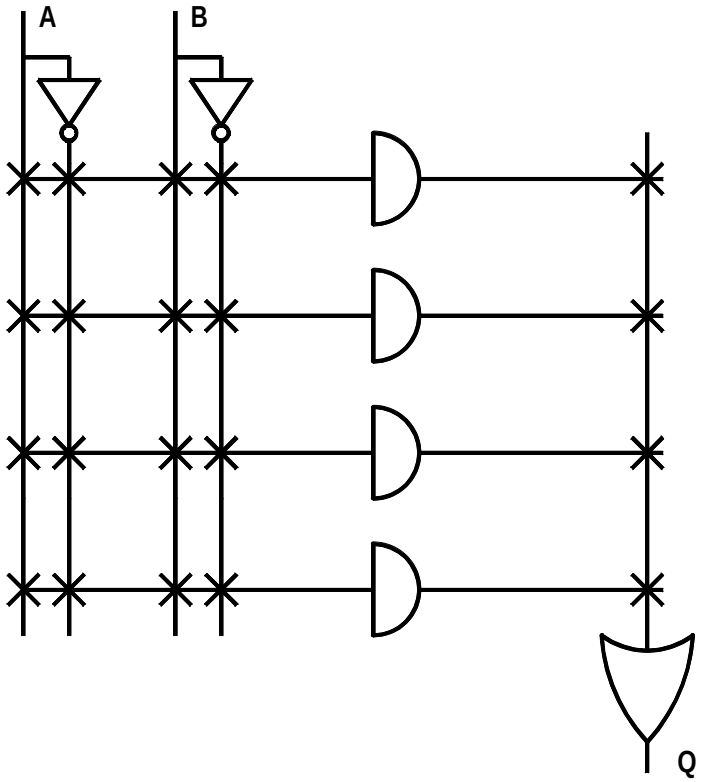
A 2 input system using a $2 \times 2 = 4$ input AND gate with all possible input signals connected through fuses.



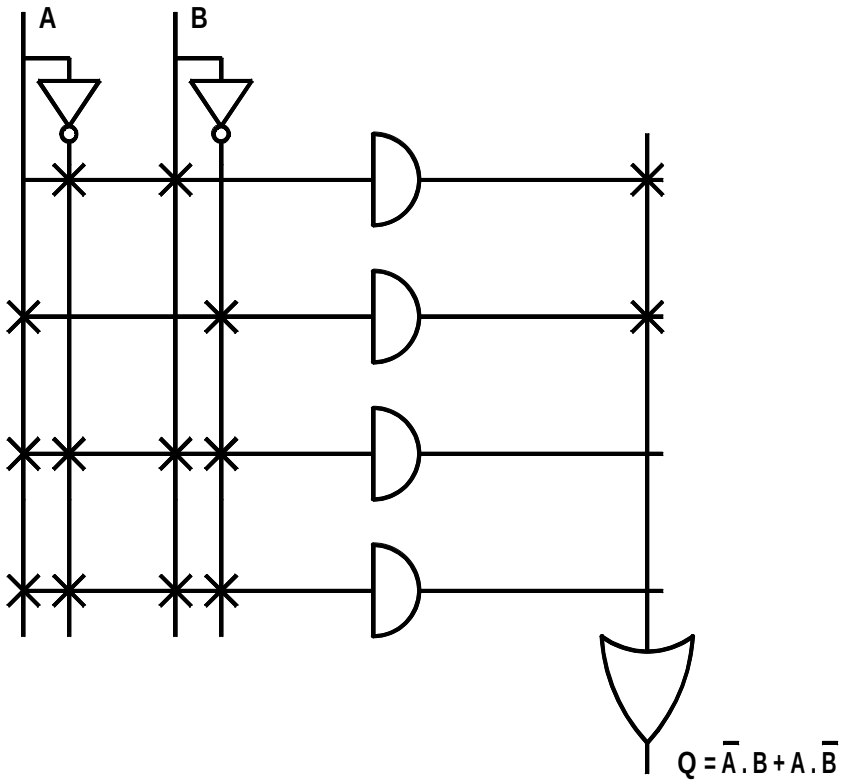
The same AND gate with two of the fuses burned out giving a logical output of $Q = \overline{A}.B$. The unconnected inputs to the AND gate default to logic 1.



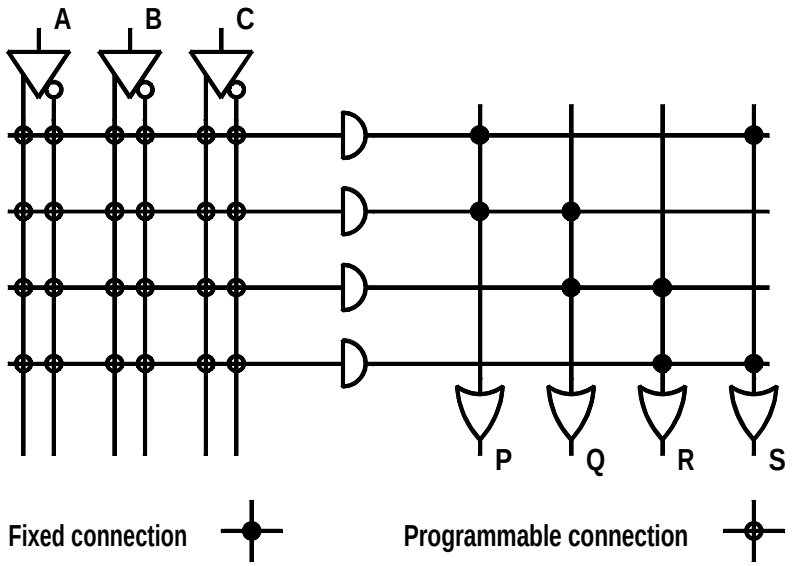
The structure which allows the implementation of any or all of the four canonical terms of the SOP formed from two inputs, A and B.



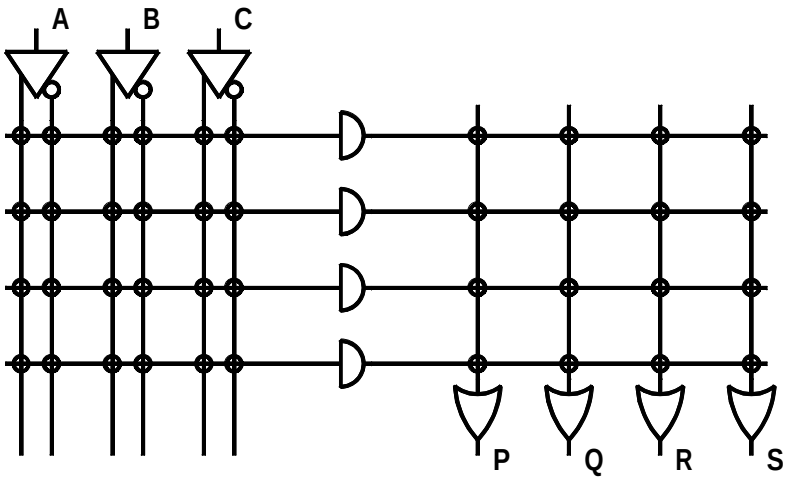
The same structure as that in Figure 21.3 but with the fusible links shown as $\times$.



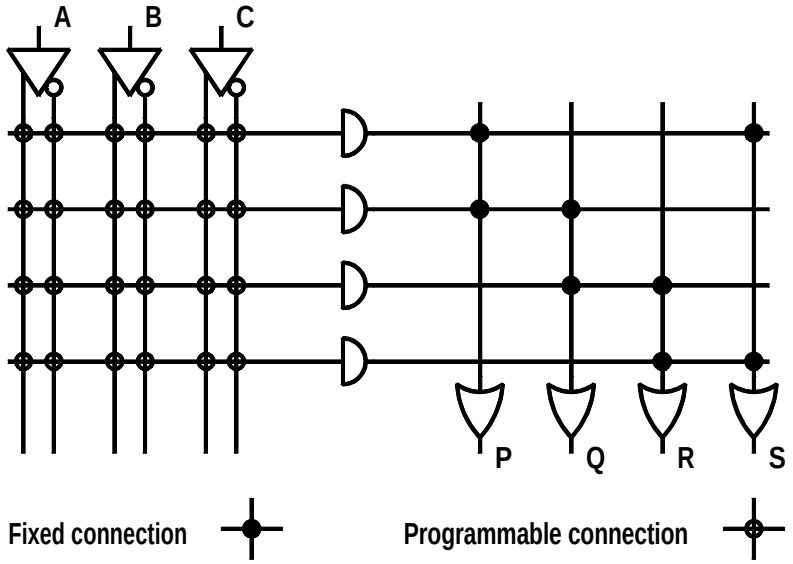
The reduced schematic for the XOR function $Q = \overline{A}.B + A.\overline{B}$.
Intact fuses are shown with an $\times$.



A Programmable Array Logic (PAL) configuration. These devices utilize CMOS technology and the links at the grid crossings are only formed when the device is programmed. The programmable links are shown with a circle. The manufactured-in fixed links are shown with a filled circle.



The Programmable Logic Array (PLA) configuration.



Problem 20.1. The generic PAL configuration.