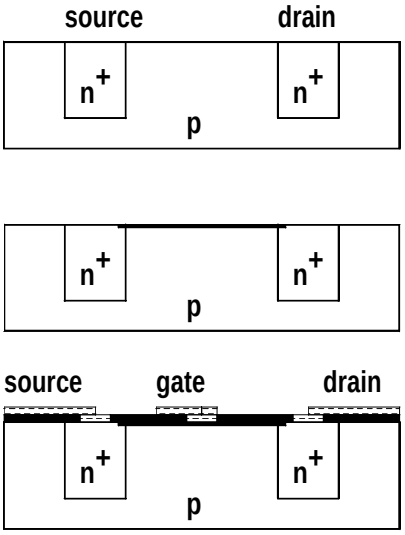
Complementary Metal Oxide Silicon.

- Uses complementary MOSFETs.
- Voltage controlled devices.
- Low power.



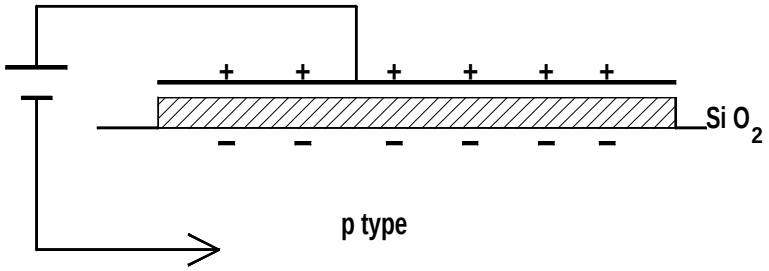
Two heavily doped (+) n type wells called source and drain are formed in lightly doped p type substrate

A thin layer of oxide is formed over the channel region

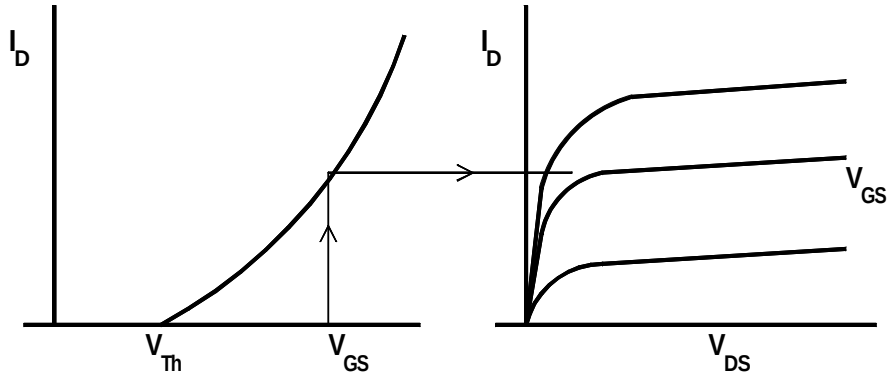
A metal gate electrode is applied over this thin oxide layer on the channel.

A covering oxide layer is applied and windows etched in oxide. Metallic contact tracks are laid down to make contact to the source, gate electrode and drain

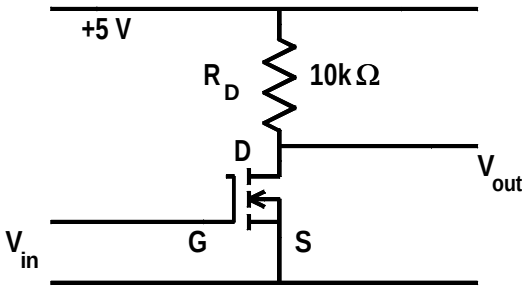
Structure of enhancement mode n channel MOSFET.



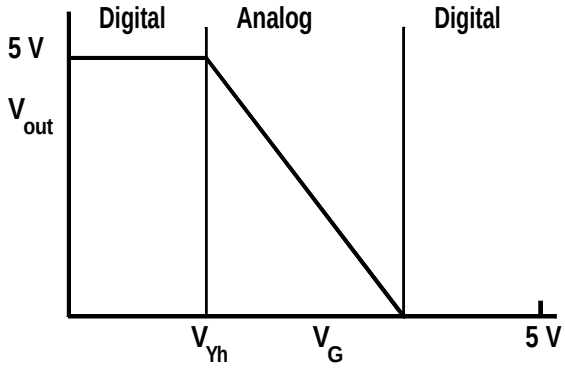
Charge layers associated with MOSFET channel enhancement.



Enhancement mode MOSFET characteristic curves.

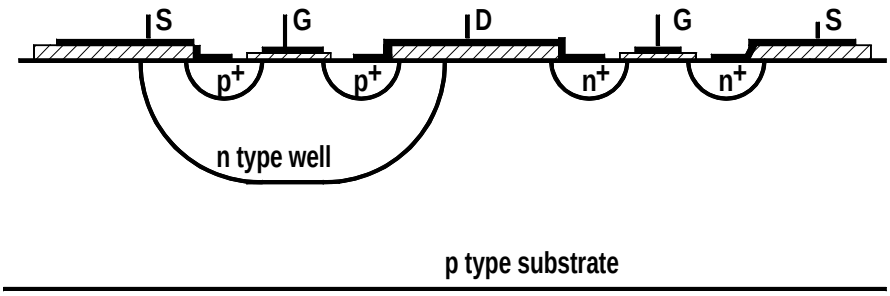


MOSFET inverter.

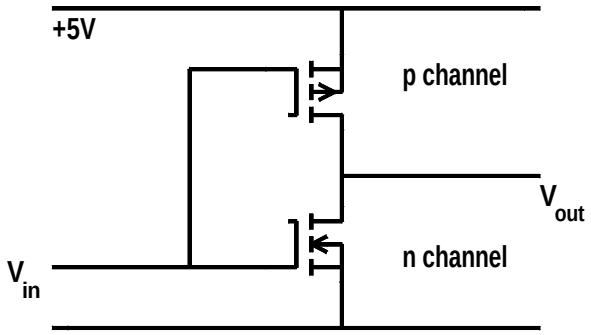


Switching characteristic of MOSFET inverter.

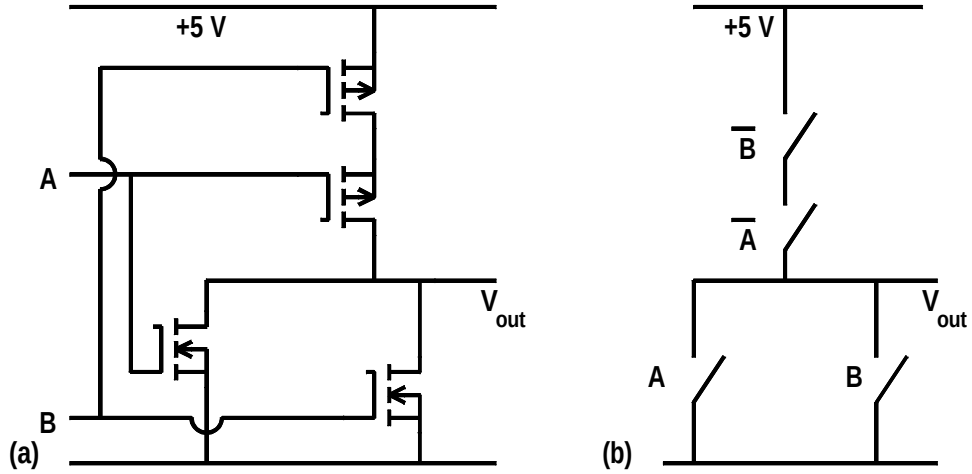
V_{in}	Logic in	Logic out	V_{out}
$< V_{Th}$	0	1	+5 V
$> 2V_{Th}$	1	0	0 V



CMOS fabrication on a wafer.

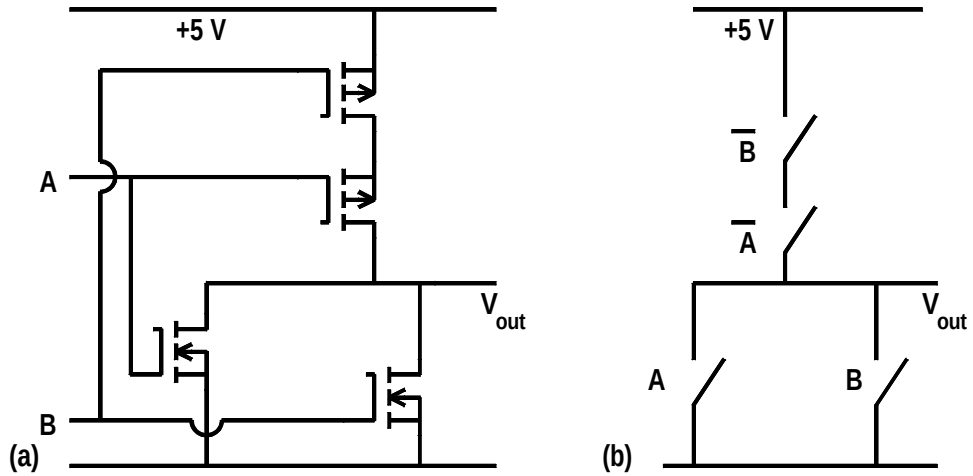


CMOS invertor.

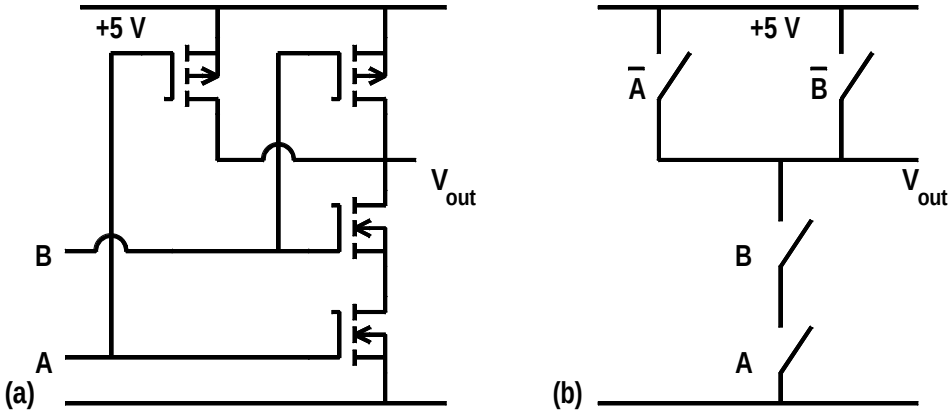


CMOS NOR gate and its switch equivalent.

A	B	A	B	Logic out	V_{out}
Open	Open	0	0	1	5 V
Open	Closed	0	1	0	0 V
Closed	Open	1	0	0	0 V
Closed	Closed	1	1	0	0 V

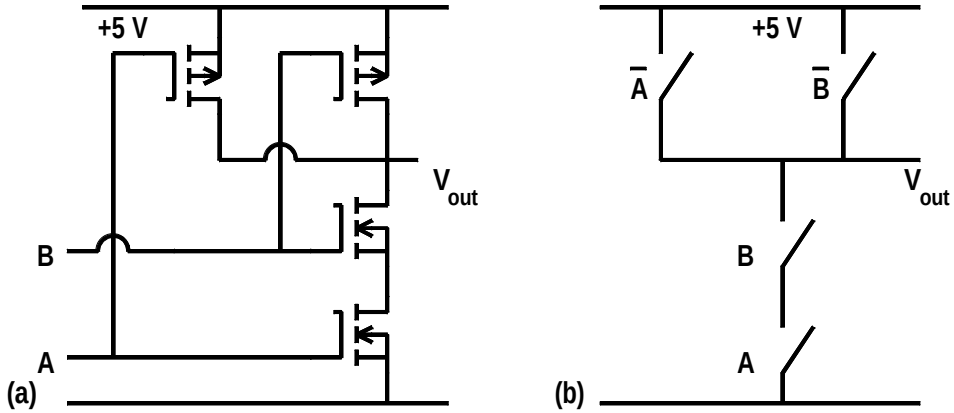


A	B	A	B	Logic out	V_{out}
0 V	0 V	0	0	1	5 V
0 V	+5 V	0	1	0	0 V
+5 V	0 V	1	0	0	0 V
+5 V	+5 V	1	1	0	0 V



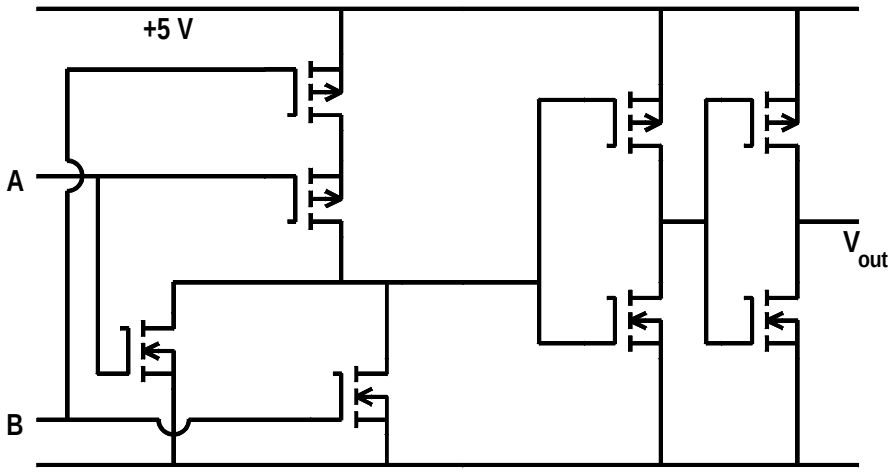
CMOS NAND gate and switch emulation.

A	B	A	B	Logic out	V_{out}
Open	Open	0	0	1	5 V
Open	Closed	0	1	1	5 V
Closed	Open	1	0	1	5 V
Closed	Closed	1	1	0	0 V

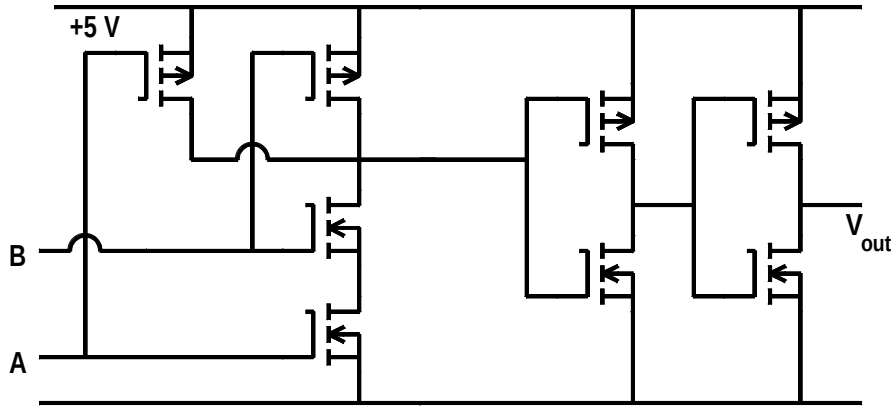


CMOS NAND gate and switch emulation.

A	B	A	B	Logic out	V_{out}
0 V	0 V	0	0	1	5 V
0 V	+5 V	0	1	1	5 V
+5 V	0 V	1	0	1	5 V
+5 V	+5 V	1	1	0	0 V



Buffered output NOR gate.



Buffered output NAND gate.