1 TTL NAND Gates

Install a 7400 two input NAND gate on the breadboard. Look up the pin assignments in the data sheet. Apply the Ground and +5 V supply to the appropriate pins. Connect the inputs and outputs of one of the NAND gates on the chip to the led displays. Then connect the inputs to the test switches so that the input and output signals are displayed on the leds.

1. Record whether the led displays are ON or OFF in a table, for all possible combinations of inputs. Deduce the truth table for the NAND gate from this test table and draw the truth table. Record the circuit which you use in your notebook together with the pin numbers.

Input A	Input B	Output

A	B	Q

   a) Record whether led ON or OFF and b) Draw up truth table for NAND Gate

2. How many NAND gates are there on the 7400 IC? What are the pin numbers for the gates? Do all of the gates work?

3. Does connecting an input to ground affect the output?

4. Does connecting an input to +5 V affect the output?

5. What is the effect of leaving an input unconnected?

6. How can you make an AND gate if you only have 7400 NAND chips available? Draw the circuit. Build it and obtain the truth table.

7. How can you make a 4 input NAND gate if you only have 7400 2 input NAND gate ICs available? Draw the circuit and build and test the circuit. Record the truth table and also record the readings at the intermediate points in your truth table. How many rows are there be in the truth table for this four input NAND gate?

8. Apply a voltage signal from a variable voltage supply and measure the input voltage which causes the output of the NAND gate to switch for both increasing and decreasing input voltages. Is there any hysteresis in this switching action? What is hysteresis?

9. Replace the NAND gate circuit which you constructed in Q7 by a 7420 Dual Four input NAND gate and test this gate. Draw the truth table. Is it the same as the truth table which you prepared in Q7.

2 TTL NOR Gates

Install a 7402 two input NOR gate on the breadboard. Look up the pin assignments in the data sheet and apply the Ground and +5 V supply to the appropriate pins. Connect the inputs and outputs of one of the NOR gates on the chip to the led displays. Then connect the inputs to the test switches so that the input and output signals are displayed on the leds.

1. Record whether the led displays are ON or OFF in a table for all possible combinations of inputs. Deduce the truth table for the NOR gate from this test table and draw the truth table. Record the circuit which you use in your notebook together with the pin numbers.

Input A	Input B	Output

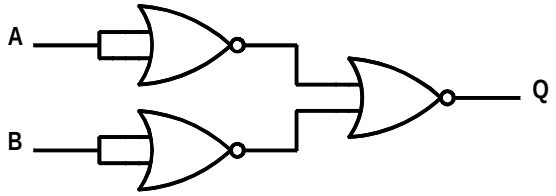
A	B	Q

a) Record whether led is ON or OFF and b) Draw up truth table for NOR gate

2. How can you obtain an OR function by using NOR gates? Draw the circuit. Build it and obtain the truth table.

3. How can you build a three input NOR gate using two input NOR gates. Draw the circuit. Build and test the circuit. How many rows are there in the truth table for this three input NOR gate?

4. Determine the truth table for the NOR gate circuit shown below



5. A seat belt warning system is required to sound a warning unless all passengers and the driver have their seat belts fastened. The warning should only sound when the ignition switch is turned on. Each seat has a weight sensor and an unfastened seat belt for an empty seat will not cause an alarm. Assign the following:
SS = Ignition Switch ON
SB1 = Driver's seat belt fastened.
SB2, SB3, SB4 = Passenger seat belts fastened.
W2, W3, W4 = Weight sensed on seats 2,3,4.

3 CMOS Gates

CMOS (Complementary Metal Oxide Silicon) gates have many advantages over the older ttl gates. The advantages include:

- The inputs to these gates are voltage driven. There are none of the problems associated with current sinking that occur with ttl gates.
- CMOS operates with a supply voltage from about 3 V to 15 V.
- Current consumption is very small. They are suitable for battery operation.
- The input voltage threshold for logic changes is at half the supply voltage.
- The output voltage will swing from 0 V to the supply voltage if the load is large.
- The CMOS 4000 series has a much greater range of logic, counting and arithmetic functions than are available in the ttl 7400 series.

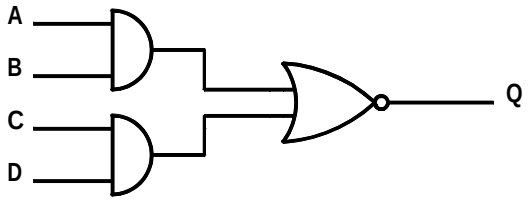
Use a CMOS 4011 Quad Two Input NAND gate or a CMOS 4001 Quad Two Input NOR gate and look up the pin assignments in the data sheet provided. Apply power to the appropriate pins. $V_{DD} = +5\,V$ and $V_{SS} = 0\,V$.

1. Are the power supply pins the same as those for the corresponding ttl IC?
2. Does the output of the 4011 drive the indicator leds on the board?
3. Obtain the truth table for the 4011 or the 4001 IC.
4. Drive one input from a variable voltage supply and record the output as a function of the input voltage.
5. Measure the output voltage for logic 0 and logic 1 output. How does this output voltage vary as the power supply voltage is changed within the permissible range?
6. Does an unconnected input default to a logic 1 or to a logic 0 or does it switch randomly depending on electrical pick-up at the input pin?
7. Is it necessary to connect all unused inputs to either logic 1 or logic 0?

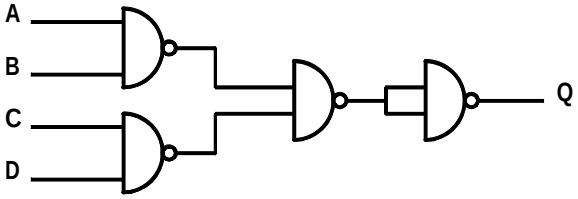
From now on this manual will refer to LOGIC gates and the options of using either CMOS (4000 series) or ttl (7400 series) will depend on availability and application. You should remember that the pin assignments may be different in the two logic families. Also a +5 V supply will operate both types. WARNING— you should not mix ttl and CMOS ICs in the same circuit. Special care must be taken to interface the two types if reliable operation is to be obtained.

4 AND-OR-INVERT Gate

The circuit for the AND-OR-INVERT function is shown in the diagram below.

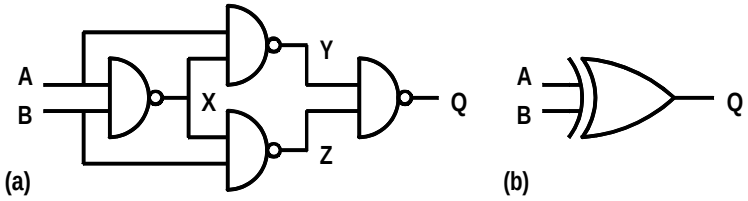


1. Construct this circuit using either CMOS (4081 AND and 4001 NOR) gates or ttl (7408 AND and 7402 NOR) gates.
2. Determine the truth table for the circuit and record it in your notebook.
3. Describe the truth table in words.
4. Suggest an example of an application of this AND-OR-INVERT circuit.
5. Is the circuit shown below equivalent to the AND-OR-INVERT circuit?

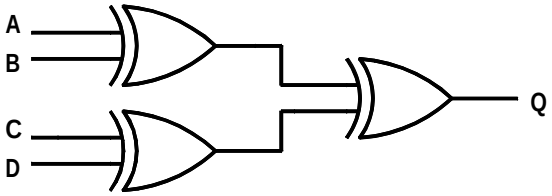


5 XOR eXclusive OR gates

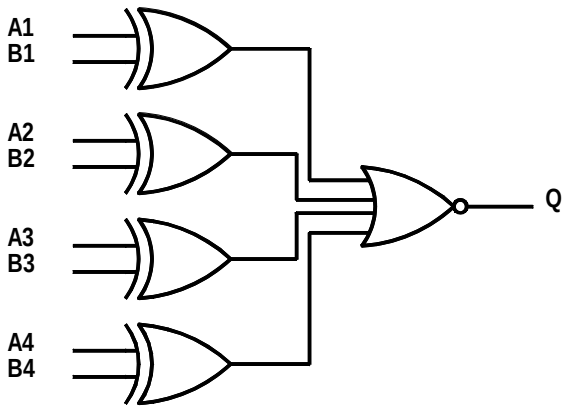
The Exclusive OR gate can be constructed using NAND gates as shown in the circuit below (a). The symbol for the XOR gate is also shown (b).



1. Build the XOR gate from NAND gates, as shown.
2. Determine the truth table and record your results in your lab book.
3. Describe this truth table in words.
4. Construct the XOR gate circuit shown below using 4070 XOR ICs (or 7486 if no 4070 are available).



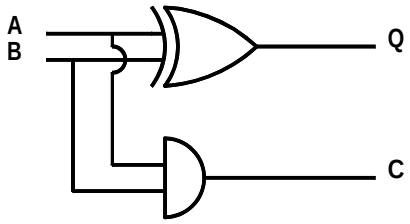
5. Determine the truth table for the circuit.
6. Describe the function of the circuit in words.
7. For what combination of input signals will a logic output of Q = 1 be obtained from the circuit shown below?



8. If this circuit were constructed from NAND gates, how many NAND gates would be needed?

6 Logic operations

1. This circuit implements what is called a "Half Adder". What is the truth table for this circuit?



2. What are the CMOS IC type numbers used in building this circuit?

3. Use a CMOS 4008B Full adder (or a 74283 ttl Full Adder) and determine the truth table of a full adder.

4. Explain the function of a full adder in words.

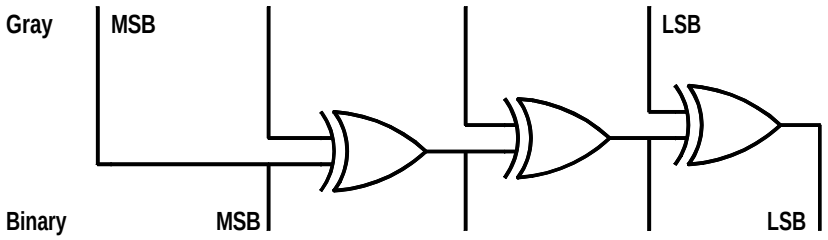
5. How many rows are there in the truth table of a 4 bit binary full adder?

6. Why do you not need to enumerate all possible input combinations in order to determine the operation of the full adder?

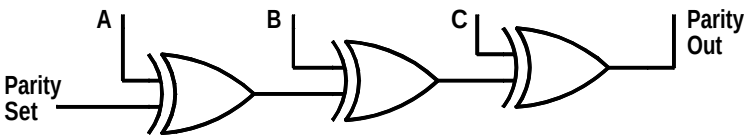
7. Add 0011_B to 0010_B with a carry in of 0.

8. Add 0101_B to 1011_B with a carry in of 1.

9. Construct the following circuit for converting Gray code to Binary code and verify the correct operation of the circuit.

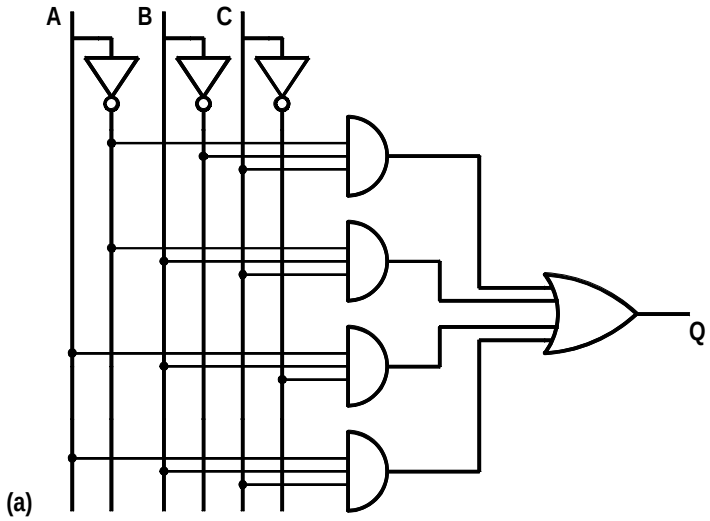


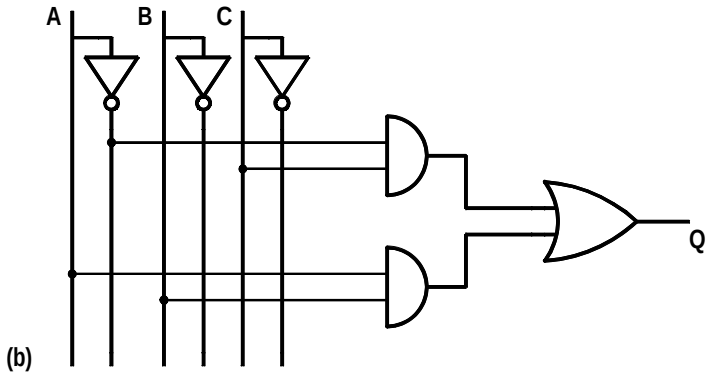
10. The XOR gates can be used to generate a parity bit as shown in the circuit below. The Parity Set is 0 for Even Parity and 1 for Odd parity. The data inputs (from switches) ar at A, B and C and the generated Parity Bit is at P. Verify the operation of the circuit for various input combinations.



7 Canonical Forms

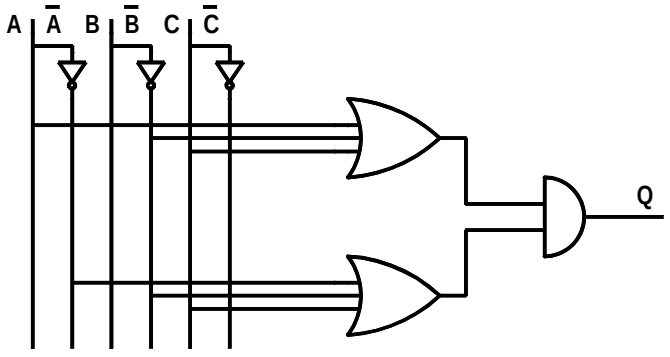
1. Connect up the two circuits shown below and show that they have equivalent truth tables. (4082 4-input AND, 4071 2-input OR). (4072 4-input OR no longer available in DIL package).





2. What are the Boolean expressions for the circuits shown above?

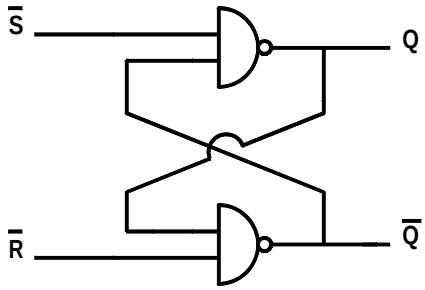
3. Connect up the circuit shown below and determine the truth table.



4. What is the Boolean expression for this circuit?

8 Latches and Flip-Flops

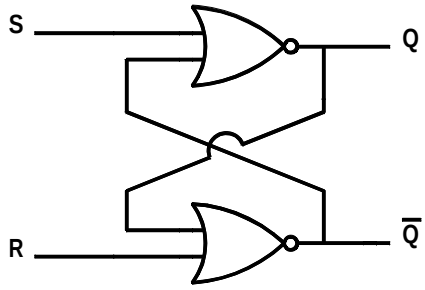
1. Connect up the NAND gate RS Flip Flop circuit circuit shown below and verify the truth table for the latch. Take care to note the output state of the latch before applying a signal so that you can identify any changes of state.



$\overline{R}$	$\overline{S}$	Q	$\overline{Q}$
1	1	Q	$\overline{Q}$
1	0	1	0
0	1	0	1
0	0	?	?

2. Is there any set of inputs for which both of the outputs Q and $\overline{Q}$ are the same?

3. Connect up the NOR gate RS latch shown below and examine the truth table.



R	S	Q	$\overline{Q}$
1	1	?	?
1	0	1	0
0	1	0	1
0	0	Q	$\overline{Q}$

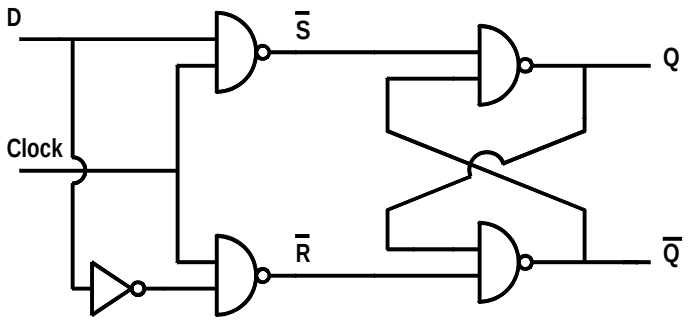
4. Connect up the D flip flop shown in the circuit below and observe the timing diagram for the Flip Flop.

5. Connect the square wave generator on the board to the clock input and set J = K = 1. Observe the rate of the switching of the output Q.

6. Compare the operation of your circuit to the operation of the 4027 JK Flip Flop.

7. Are the IC versions positive or negative edge triggered devices?

8. How will the type of device (positive or negative edge triggered) affect the timing waveforms which you observe with an oscilloscope?



9. What happens when the Q output of one is connected to the clock input of another and the control are J = K = 1 for each?

9 Binary and BCD Counters

1. Connect up a binary counter (either a 4024 7 stage binary counter or a 4040 12 stage binary counter) and apply a slow clock to the clock input. Display the outputs of the stages on the leds. Observe the switching of the leds.

2. It is necessary to apply a logic 0 to the Reset in order to make the counter count.

3. What happens to the display if the Reset is brought to logic 1 while counts are shown on the display?

4. Increase the rate of the clock connected to the input and observe the waveforms at the outputs using an oscilloscope. Sketch the waveforms and prepare a timing diagram.

5. Connect a 4029 BCD counter and apply a slow clock to the input. For normal counting operation, what signals should be applied to the Carry In, Reset and Load inputs? Configure the counter to count up. Note the sequence of the led indicators.

6. Change the configuration to make the counter count down. Note the changes in the sequence of the output signals.

7. Apply a valid BCD code to the L1, L2, L3 and L4 inputs and bring the Load input to Logic 1 for a short time. The count will then resume from this preloaded value.

8. How would you use the counter to count 6 bean cans into a box on a production line and then trigger the conveyor belt advance to the next box? Draw a possible circuit for the controller.